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論文

3次元実装に用いる高アスペクト比貫通電極の銅穴埋めめっき

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Copper Via Filling Electrodeposition of High Aspect Ratio Through Chip Electrodes Used for the Three Dimensional Packaging

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Abstract

Through chip electrodes with high aspect ratios used for three dimensional packaging can offer the shortest interconnection and reduce signal delay. Copper has good compatibility to conventional multi layer interconnection in LSI and BEOL (back end of line process). In this work, filling vias with higher aspect ratio, 10 μm in square and 70 μm in depth, used for through chip electrodes was investigated. Removing overhang at via top is important to achieve perfect via fill of 10 μm in square and 70 μm in depth. With testing a series of electrodeposition conditions, conformal electrodeposits were obtained. With those conformal electrodeposits, seams and voids always remain at the via center. Perfect via filling without seams or voids was achieved by increasing leveler of JGB concentration to 30 mg/L. The electrodeposition time was reduced to 3.5 hrs by using two steps pulse reverse current.

Key Words: *Three Dimensional Packaging, Through Chip Electrode, Via Filling, Pulse Reverse Current, Additives, Electrodeposition*