

Call for Papers

ICEP 2016

2016 International Conference on Electronics Packaging

April 20-22, 2016

Sapporo Education and Culture Hall, Hokkaido, Japan

Sponsored by JIEP, IEEE CPMT Society Japan Chapter and IMAPS

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Technical Topics and Keywords for Conference Papers

1. Advanced Packaging

Wafer Level Packaging, System Integration, PoP, MCM, System on Package, Novel Assembly Technologies

2. Substrates and Interposers

Laminates, Interposers, Fine Pitch, Build-Up Substrates, Flexible Printed Circuits, Embedded, Conductive Paste, Thin Core, Coreless, Low CTE

3. Interconnection

Bump Formation, Chip-Package Interaction, Low k, Leadframe, Test of First- and Second- Level Interconnections, Interconnections for 3D Integration, Interconnections in Substrates, PCBs and Systems

4. 3DIC Packaging

TSV, Via Formation and Filling, 2.5D, Wafer Thinning, Silicon Stacking, Chip on Chip, Chip on Wafer, Wafer on Wafer, Wide Bus, Wireless Interconnection, Temporary Bonding/De-Bonding

5. Design, Modeling, and Reliability

Signal and Power Integrity, High-Speed Board Design, Mechanical Design and Reliability, Failure Analysis, Fracture and Warpage in Packages, Testing, Evaluation, TCAD, 3DIC Design

6. Thermal Management

Advanced Cooling Modules, Heat Pipes, Heat Sinks, Fans and Blowers, Thermal Interface Materials, Thermal Measurements, Micro and Nano Scale Heat Transfer, Thermal Issues in Devices

7. Materials and Processes

Novel Materials and Processing, Dielectrics, Emerging Materials and Processes for 3D, Thin Films, Underfills, Assembly Challenges and Solutions, Wafer Thinning, Plating, Equipment, Encapsulation

8. Printed Electronics

Inkjet, Screen Printing, Conductive Wiring, Insulation, Printed Organic TFTs, Device Applications

9. N-MEMS

NEMS-MEMS/Sensor Devices, MOEMS, Assembly and Packaging, Nano Technology, Nano Imprint Lithography, Organic Semiconductors, Wireless Sensor Networks

10. Optoelectronics

Active Optical Cable, Photonic Devices, Optical Fibers, Waveguides, Optical Interconnects, Transceivers, Connectors, LD/PD, LED, OE/EO, TOSA/ROSA, WDM, Optical Wiring Boards

11. Self-Organization/Self-Assembly

Biomimetics, Nature-Guided, Bottom-Up Manufacturing, Smart Materials and Devices, Spontaneous Ordering/Patterning/Structuring, Self-Bonding/Debonding, Repairable, Self-Healing, Novel Micro/ Nano Processing

12. Medical Devices

Invasive, Low Invasive, Non Invasive, In Vitro, BAN, Cure, Treatment, Diagnosis, Screening, POC, Healthcare

13. Power Electronics Integration

Si, SiC or GaN Power Device/Module Packaging and Reliability; Packaging of High-temperature Power Electronics, Sensors; Inverters/Converters for Electric Vehicles; Magnetic Materials and Components; PE Substrate Technologies; PE Encapsulation Materials; PE Integration by 3D Printing

14. RF

RFID, High Frequency Devices, Packaging, Filters, EMI, EMC, Antennas, Wireless Power Transmission

15. Others

 $\label{thm:market} \mbox{Market Trends, Environmentally Conscious Products and Processes, Cost Analyses}$

Conference Information

Registration Fees:

Member of JIEP / IEEE / IMAPS: 41,000 yen (including reception and the proceedings)

Non Member: 55,000 yen (including reception and the proceedings)

Students: 12,000 yen (including the proceedings)

Organizing Committee:

General Chair: J. Mizuno, Waseda University General Vice Chairs: S. Uegaki, ASE Group; Y. Nogami, Toray Engineering; K. Yokouchi, Fujitsu Interconnect Technology

Contact:

Secretariat of ICEP 2016

The Japan Institute of Electronics Packaging

E-mail: icep2016@jiep.or.jp URL: http://www.jiep.or.jp/icep/

Abstract Preparation

A 300-word abstract to be submitted to the web site below by **October 31, 2015.**

http://www.jiep.or.jp/icep/

Authors are requested to attach a figure, a picture or a table. Notification of acceptance by the middle of December, 2015.

Final manuscript of four to six pages should be submitted by February 20, 2016, for both oral and poster presentations.

Accepted and presented papers will be published in the conference proceedings and submitted to IEEE Xplore.





