	Room A (605-606)	Room B (607)	Room C (608)	Room D (610)
9:00 10:40	**FA1: 3D-3** **FA1-1** <Session Invited> Necessity of Chip on Chip Technology for 3D IC Hiroshi Ozaki, Sony / Japan **FA1-2** Encapsulation Technology by Silicon Based Cavity with TSV Electrode for Pseudo-SoC Application Toshihiko Nagano, Kazuhide Abe, Hiroshi Yamada, Kazuhiko Itaya, Toshiba / Japan **FA1-3** Wafer-level Over molding Process Development for a stacked WCSP Package with Through Silicon Via (TSV) Yoshimi Takahashi, Texas Instruments / Japan **FA1-4** Development of Si Interposer for 2.5D Advanced Package Satoru Kuramochi[1], Yoshitaka Fukuoka[2], [1]Dai Nippon Printing [2]World wide Electronic Integrated Substrate Technology / Japan	**FB1: Advanced-1** **FB1-1** <Session Invited> *(50min.)* Development of High-end CPU Packaging for Supercomputer Masateru Koide, Fujitsu Advanced Technologies / Japan **FB1-2** Wafer level packaging to address future direct chip attach needs Yoshihiro Tomita, Intel K.K. / Japan **FB1-3** Analysis on design and mechanical stress of 2.5D package interposers Takashi Hisada, Toyohiro Aoki, Junko Asai, Yasuharu Yamada, IBM Japan / Japan	**FC1: Interconnection-1** **FC1-1** Adhesion test for underfill delamination in flip chip package Keishi Okamoto, IBM Japan / Japan **FC1-2** Interfacial phenomena in barrier layer SiCN / Cu film related to adhesion Satoko Abe, Teruhisa Baba, Kenichi Ueoka, Kouji Yoneda, Jiping Ye, NISSAN ARC / Japan **FC1-3** Effect of the crystallinity of electroplated copper thin films on their mechanical and electrical reliability Naokazu Murata, Tohoku University / Japan **FC1-4** Die Pull Tester for Flip-Chip Bonding Yoshiyuki Arai, Toray Engineering / Japan	**FD1: DMR-3** **FD1-1** Reliability Study of Thick-film Pressure Sensor on Steel Substrate Zongyang Zhang[1,2], Sheng Liu[1,2], [1]Huazhong University of Science & Technology, [2]Wuhan National Laboratory for Optelectronics / China **FD1-2** A Thermal Model for Non-linear Distortion in Printed Circuit Lines for Condition Monitoring of Electronics Michael Krüger[1], Nils F. Nissen[2], Herbert Reichl[1], Klaus-Dieter Lang[1], [1]Technische Universitaet Berlin, [2]Fraunhofer IZM / Garmany **FD1-3** An Analysis of Failure of Microelectronic Packaging due to Conductive Anodic Filament Formation Jan-Long Yang, Mei-Ling Wu, National Sun Yat-Sen University / Taiwan (10:15)
	Break			
10:50 12:30	**FA2: Korea Session-1** **FA2-1** Wetting characteristics of Cu-xZn layers for Sn-3.0Ag-0.5Cu solders Ji Hyun Lee, Young Min Kim, Young-Ho Kim, Hanyang University / Korea **FA2-2** Cost Effective Coreless Process for Thinner Substrate Hwa Dong Oh, Young Joo Ko, Daeduck Electronics / Korea **FA2-3** A Novel High-Efficient Aligning Structure for Optical PCB Interconnection Dongmin Kim, Pusan National University / Korea **FA2-4** The Effects of Levelers on 3D SiP Copper Via Filling Myung-Won Jung, Ki-Tae Kim, Jae-Ho Lee, Hongik University / Korea	**FB2: Advanced-2** **FB2-1** Low Cost fcCSP Based on Cu Pillar Bernd Karl Appelt, ASE Group / USA **FB2-2** Thin SiP and 3D eWLB Technology for Advanced Packaging Seung Wook Yoon, STATS ChipPAC / Singapore **FB2-3** Novel EMI Shielding Methodology on SiP Module Kuo-Hsien Liao, Advanced Semiconductor Engineering / Taiwan **FB2-4** A Double Die DRAM Package Optimized For PTH PCB use in UltraBook™ and Tablet PC Applications Richard D. Crisp[1], Wael Zohni[1], Bel Haba[2], [1]Invensas, [2]Tessera / USA	**FC2: MFG-3** **FC2-1** Wire Sweep Analysis for Copper Wire and Pd-coated Copper Wires in Semiconductor Wirebonding Technology Huang-Kuang Kung[1], Ming-Cheng Lu[1], Che-Chang Li[1], Hong-Meng Ho[2], [1]Cheng Shiu University / Taiwan, [2]Semicon Fine Wire Pte / Singapore **FC2-2** Flip-chip Interconnection by Pre-applied Under-fill Material Using Copper Pillar Bumps Hiroki Maruo, Koji Motomura, Hideki Eifuku, Tadahiko Sakai, Panasonic Factory Solutions / Japan **FC2-3** B-stageable no-flow underfill for fine pitch die to substrate packages Kenichi Tosaka, Namics / Japan **FC2-4** Flux Residue Cleaning Process Optimization for Flip Chip Ball Grid Array (FCBGA) Noor Azrina Talik, Univeriti Tenaga Nasional / Malysia	**FD2: DMR-4** **FD2-1** Innovative 4Layer CPU Package Design to Enable Low Cost Platform Solution Chan Kim Lee, Chin Lee Kuan, Howe Yin Loo, Intel Microelectronics (M) / Malysia **FD2-2** Walkthrough on Package Design Challenges, Optimization and Technical Resolutions Howe Yin Loo, Chan Kim Lee, Intel Microelectronics (M) / Malysia **FD2-3** An Innovative Motherboard Concept to Enable Low Cost Package Decoupling Solution Howe Yin Loo, Chan Kim Lee, Intel Microelectronics (M) / Malysia **FD2-4** A New Proposal for Representing the Process of Electronics Packaging Using DSM Keiichi Ohizumi, Atsushi Maeda, O2 / Japan
	Lunch			
13:30 15:10	**FA3: Korea Session-2** **FA3-1** Characteristics of Heat Dissipation and Light Output Power of High-Power LED Packages Processed with Various Thermal Via Technologies Min-Young Kim[1], Byung-Kyu Yu[1], Tak Jeong[2], Jun-Seok Ha[3], Tae-Sung Oh[1], [1]Hongik University, [2]Korea Photonics Technology Institute, [3]Chonnam National University / Korea **FA3-2** Electrical Properties of Polymer Solar Cells with PCDTBT:PCBM Active Layer Kun Ho Kim[1], Seung Ho Kim[1], Young Chul Chang[2], Ho Jung Chang[1], [1]Dankook University, [2]Korea University of Technology and Education / Korea **FA3-3** Underfill Thermal and Mechanical Model Study with Filler Variation Woongsun Lee, Hynix Semiconductor / Korea **FA3-4** Abrasion Resistance of Nano Crystal Ni plated on Mold Cavity Yongbin Sun, Kyonggi University / Korea **FA3-5** Cancel (15:35)	**FB3: Advanced-3** **FB3-1** <Session Invited> Key Packaging Technologies Progressing Fast This Year Hirofumi Nakajima, Renesas Electronics / Japan **FB3-2** Formic gas used Cu surface treatment and low temperature direct bonding Wenhua Yang, Masatake Akaike, Tadatomo Suga, The University of Tokyo / Japan **FB3-3** Impact of the oxidation process on copper leadframe surface causing delamination between copper and mold compound interface Chin Yung Lai, Infineon Technologies / Malysia **FB3-4** Copper Wire Bonding is a Viable Interconnection Method Bernd Karl Appelt, ASE Group / USA	**FC3: Thermal-2** **FC3-1** Industrial need for accurate and reproducible measurements of thermal interface materials Andras Vass-Varnai[1,2], Zoltan Sarkany[1,2], Marta Rencz[1,2], [1]Budapest University of Technology and Economics, [2]Mentor Graphics / Hungary **FC3-2** Developing preferential heat flow path in metal matrix composite Makoto Kobashi, Naoyuki Kanetake, Nagoya University / Japan **FC3-3** Steady and transient thermal simulation of GaN devices for high-speed switch application Satoshi Ono[1], Shigeru Hiura[1], Mauro Ciappa[2], Wolfgang Fichtner[2], [1]Toshiba, [2]Swiss Federal Institute of Technology / Japan **FC3-4** Development and analysis of the thermoelectric material with intermetallic compound Li-Ling Liao[1,2], Ming-Ji Dai[1], Chun-Kai Liu[1], Jing-Yao Chang[1], Kuo-Ning Chiang[2,3], [1]Industrial Technology Research Institute, [2]National Tsing Hua University, [3]National Center for High-Performance Computing / Taiwan	**FD3: DMR-5** **FD3-1** On-die PDN Response Observation of a 6.4Gbps SerDes Device by Direct Excitation from an External Signal Source and the System-Level PDN Modeling Masahiro Toyama, Ryuichi Oikawa, Motoo Suwa, Atsushi Nakamura, Renesas Electronics / Japan **FD3-2** Characterization of Electromagnetic Noise Coupling in DC-DC Converter Module Keisuke Sawada, Masaya Tanaka, Shuji Sagara, Tatsuya Ikeuchi, Dai Nippon Printing / Japan **FD3-3** Icc(t) Modeling Methodology for High Speed DDR Power Integrity Design Heng Chuan Shu, Fern Nee Tan, Intel Microelectronics (M) / Malysia **FD3-4** Does Power Rail Merger work for High Speed I/O interfaces like PCIe, SATA and USB? Fern Nee Tan, Intel Microelectronics (M) / Malysia
	Poster Core Time			
15:40 17:20	**FA4: Interconnection-2** **FA4-1** <Session Invited> *(50min.)* Achieving Fine Geometry Through Embedded Fabrication & Assembly Chuck Bauer, TechLead Corporation / USA **FA4-2** Improvement of Low-k Delamination with Substrate Pad Structure for Lead-Free Package Makoto Okada, Michihiko Ichinose, Kouji Kimbara, Renesas Electronics Corporation / Japan **FA4-3** A Unique Low-Ag Alloy Solder Paste for High-Reliability SMT Applications Masato Shimamura, Senju Metal Industry / Japan **FA4-4** An acceleration model with thermal cycle profile for Pb-free solder joint reliability Akifumi Yoshimura, Keishi Okamoto, IBM Japan, / Japan	**FB4: Substrate** **FB4-1** Challenges to Increasing Wiring Density for Organic Packaging Substrates Masahiro Tsuriya, Haley Fu, iNEMI / Japan **FB4-2** Interposer-embedded packaging technology, a feasible solution for thinner form-factor Yu-Wei Huang, Ren-Shin Cheng, Yin-Po Hung, Fang-Jun Leu, Pei-Cheng Chang, Tao-Chih Chang, Tai-Hong Chen, Industrial Technology Research Institute / Taiwan **FB4-3** Advanced Low CTE Organic Package Material for Chip Scale Packaging Masahiro Fukui[1], Tomoyuki Yamada[1], Kenji Terada[1], Yoshihiro Hosoi[1], Masaaki Harazono[1], Teruya Fijisaki[1], Francesco Preda[2], Jean Audet[2], Sushumna Iruvanti[2], Shidong Li[2], Scott Moore[2], Charles Reynolds[2], [1]KYOCERA SLC Technologies / Japan, [2]IBM / USA **FB4-4** Warpage Resolution for Ball Grid Array (BGA) Package in a Fully Integrated Assembly Alvin Binza Denoyo, Cypress Manufacturing / Philippines **FB4-5** Adhesion Characteristics of Magnetron-Sputter Deposited Copper on Smooth Cycloolefin for Realizing High-Performance Printed Wiring Board Tetsuya Goto, Tohoku University / Japan	**FC4: Thermal-3** **FC4-1** Thermal Design and Implementation of Hybrid Cooling Systems for HPC Systems Jie Wei, Fujitsu Advanced Technologies / Japan **FC4-2** Transient Heat Conduction Simulation of the Microprocessor - Investigation regarding Thermal Control with Power Limiting Koji Nishi, AMD Japan / Japan **FC4-3** Thermal Transient Measurement based Thermal Distribution and Heat Spreading Path Structural Analysis Yafei Luo, Mentor Graphics / Japan **FC4-4** The Development of aHSBGA Andy Tseng, ASE / USA **FC4-5** A method of high accuracy prediction of θjb and θjc from θja through thermal network analysis Kenichi Inaba, NEC / Japan	**FD4: DMR-6** **FD4-1** Evaluation of 6.4 Gbps Single Ended Interface Through a Standard DIMM Connector Keisuke Saito, Arun Vaidyanath, Rambus / USA **FD4-2** Design and Analysis of Power Delivery Network in an SoC: A Review-Power Delivery network Li Wern Chew, Intel / Malysia **FD4-3** Extension of EOSE Method to Weak Nonlinear Systems and Its application to InGaP/GaAs HBT MMIC Parallel Tracks Hirobumi Inoue[1], Kazuhiko Honjo[2], Ryo Ishikawa[2], [1]NEC, [2]The University of Electro-Communication / Japan **FD4-4** A Novel High-Frequency Analysis and Modeling for the Printed-Circuit Board Using Enhanced Optimized Segment Extraction Method with Multi-Port S-Parameter Hirobumi Inoue[1], Kazuhiko Honjo[2], [1]NEC, [2]The University of Electro-Communication / Japan **FD4-5** Measurement and Simulation of Transmission Characteristic for Interconnect Structure Using 30μm Pitch Microbump Array on Coplanar Waveguide Yotaro Yasu[1,2], Katsuya Kikuchi[2], Fumiki Kato[2], Shunsuke Nemoto[2], Hiroshi Nakagawa[2], Kohji Koshiji[1], Masahiro Aoyagi[1,2], [1]Graduated School Tokyo University of Science, [2]Natinal Institute of Advanced Industrial Science and Technology / Japan