ADVANCED PROGRAM

ICEP2008

International Conference on Electronics Packaging

June 10(Tue)-12(Thu), 2008

Tokyo Big Sight, Tokyo, Japan

Welcome to ICEP 2008

We look forward to welcoming you to the International Conference on Electronic Packaging (ICEP) 2008 at Odaiba, Tokyo. ICEP 2008 will focus on diverse JISSO technologies in order to create tremendous possibilities for electronics materials, components, and packaging. The Organizing Committee has rescheduled the conference from April to June so that it will almost coincide with the JPCA show, which is one of the biggest electronic circuit exhibitions in Japan. This is a golden opportunity for you to get the latest information about cutting-edge technologies, including those still at the R&D stage, and to find out about newly developed products.

This annual conference, launched in 2001, is now in its eighth year. The conference covers almost all JISSO technology, from packaging materials to high-performance electronic components. Prior to 2000, we held the IEMT/IMC Symposium four times (1997-2000), following the merger of IEMT (by the IEEE CPMT Society of Japan) and IMC (by ISHM Japan). The 2008 conference will focus on advanced packaging technology for future innovative electronic products. The technical program consists of the following topics: Surface Activated Bonding, Interconnection, Advanced Packages, 3D Packaging, Materials and Processing, Substrates/Interposers, High Frequency Technology, MEMS and Sensor, Optoelectronics, LEDs, Simulation, Test and Analysis and Trend. Invited speakers from the United States and Japan will present next-generation high-density packaging technologies for today and the future. In addition to oral presentations, there will be poster sessions. The Poster Award will be introduced this year for younger presenters.

The conference will offer you a chance to network with fellow professionals in the field of JISSO technologies and in related fields. We are confident that the conference will provide excellent opportunities for participants to exchange information and network globally. We are looking forward to seeing you at the conference.

Hironori Asai
General Chairperson
ICEP 2008

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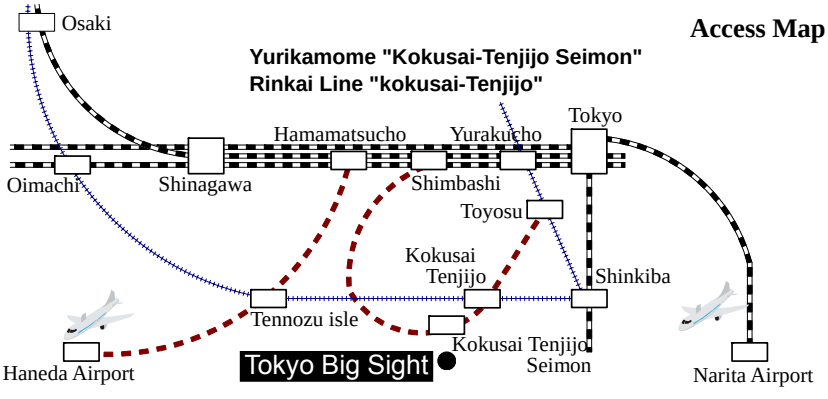
Registration Fees

Member	47 000 yen* (40 000yen)
Non Member	57 000 yen* (50 000yen)
Student	5 000 yen**
Welcome Reception Only	8 000 yen

*Including Reception and Proceedings
**Including Proceedings
( ) Advance by May 24, 2008

Access Map

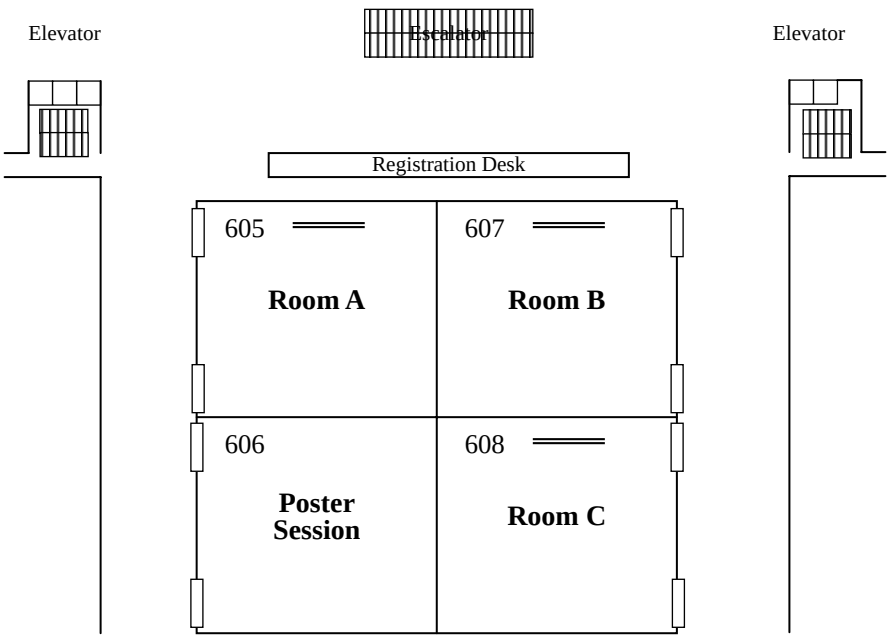


June 10

	Room A	Room B	Room C
10:00	[10A1] Surface Actuated Bonding 1. Low Temperature Bonding of CMP-Cu in Humidified Oxygen Gas at Ambient Air Pressure A.Shigetou, National Institute for Materials Science, T. Suga, The University of Tokyo / Japan 2. Influence of Surface Contamination on Low-Temperature Bonding of 20-μm-Pitch Au Micro-Bumps Y-H.Wang, T.Suga, The University of Tokyo / Japan 3. High-Precision Alignment for Wafer Bonding Using Moiré Method C.Wang, T. Suga, The University of Tokyo / Japan 4. Surface Activated Bonding for GaN/Al and Electrical Characterization of Bonded Interface A.Kaneko, E.Higurashi, M.Akaike, T.Suga, The University of Tokyo / Japan 5. Nano-Bonding for Emerging System Integration M.R.Howlader, McMaster University / Canada 6. Enhancement of the Adhesive Force of Metal Films on PTFE Surface Achieved by Fast-Atom-Beam Surface Modification S.Yamamoto, T. Kishimoto, Y. Utsumi, University of Hyogo / Japan	[10B1] Trends 1 Input Impedance Characteristics of Wearable Transmitters for Body-Centric Networks F.Koshiji, K.Sasaki, The University of Tokyo / Japan 2 Analysis of Manufacturability and Yielded Cost for Emerging Technologies C.E.Bauer, H.J.Neuhaus, TechLead / USA 3 Productization of Mobile Phone Customer Care Services T.Rantala, Nokia, A.Tuominen, University of Turku / Finland 4 Trends in Embedded Components E.J.Vardaman, TechSearch International / USA 5 Development of Fabric Antenna for Wearable Applications E.Isogai, Y.Okamoto, Musashi Institute of Technology, A.Kuramoto, T.Harada, N.Tamaki, S.Yamamoto, NEC / Japan 6 Success in Productization? J.Kantola, Tampere University of Technology, A.Tuominen, University of Turku / Finland	(10:25) [10C1] Advanced Package 1 Development of FBGA Package with Stacked Striplines for High-speed Transmission M.Maetani, T.Matsubara, K.Oda, K.Watanabe, Kyocera / Japan 2 High-Density, Wafer-Level Package Interconnect Providing a Reliable and Low-Cost Alternative to Through Silicon Vias for Image Sensors G.Humpston, Tessera / UK 3 Approach for Low-Theta-JC High-end Flip Chip BGA Y.Imaizumi, T.Suda, A.Katsumata, Toshiba LSI Package Solutions / Japan 4 Pseudo-SOC Technology: Its Basic Structure and Stress Analysis Y.Onozuka, H.Yamada, A.Iida, K.Itaya, M.Nishigaki, H.Funaki, Toshiba / Japan 5 Formation of Through Silicon Via by Bosch Process and Analysis of Seed Layer Profiles Inside the Vias C-G.Kim, D-S.Lee, B-H.Jung, W-J.Lee, KAIST / Korea
12:30			
12:30 13:30	Lunch Time		
13:30	Awarding Ceremony		
13:45	Invited Speeches 1. IC Packaging Technology Research Business Model an Industrial Partner Perspective Goal: Create an Efficient and Cost Effective Research Infrastructure Dr. Mario A. Bolanos, Texas Instruments / USA 2. 3D Chip Integration Technology using TSV's, Thin Si & Fine Pitch Interconnections for next Generation Systems Dr. John U. Knickerbocker, IBM / USA 3. Solving Issues of LSI by 3-Dimensional System-in-Package -- LSI Designer's Perspective -- Prof. Takayasu Sakurai, The University of Tokyo / Japan		
16:25			

17:00	Welcome Reception
18:30	

Conference room (605, 606, 607, 608)



Poster Session (June 11)

1 Via-filling Plating Applying to Wafer-level Chip Size Package
Y.Wakuda, I.Koiwa, Kanto Gakuin University, T.Tamura, T. amada, Noge Electronic Industries / Japan

2 Fabrication of Photo Mask by Electroless Ni-P Plating on Glass
T. Kaneda, I. Koiwa, H. Honma, Kanto Gakuin University / Japan

3 Effect of Inserted Electroless Ternary Alloy as Intermediate Films between Au and Cu pad on Wire Bondability
K. Honma, K. Yoshida, Y. Wakuda, I. Koiwa, H. Honma, Kanto Gakuin University / Japan

4 Polymer Parallel Waveguide with Graded-Index Rectangular Cores toward High-Speed On-Board Optical Interconnects
T.Kosugi, T.Ishigure, Keio University / Japan

5 Investigation of UWB Unbalanced Dipole Antenna Built in USB Memory Case
K. Nakamoto, Tokyo University of Science / Japan

6 A Study of Non-destructive Inspection System for Joint Reliability of Area-arrayed Small Bumps in 3D-stacked Flip Chip Packaging Structures
Y.Sato, H.Miura, Tohoku University / Japan

7 An Architecture of Dynamically Reconfigurable Systolic Array
T. Ishimura, A.Kanasugi, Tokyo Denki University / Japan

June 11

	Room A	Room B	Room C
9:00	(9:50) [11A1] Simulation I 1 Mechanical Modeling and Characterization of Mold Compound for Package Flatness in 3D Packages Y.Suzuki, K.Abe, M.Amagai, Texas Instruments Japan / Japan 2 Study of Minimal Condition for Package Warpage Using Visco-Elastic Calculation Tool I.Hirata, NEC / Japan 3 Implementation and Estimation of FDTD-based Electromagnetic Field Solver on Parallel Hardware N.Oguni, Y.Nakazono, K.Katayama, H.Asai, Shizuoka University / Japan	[11B1] PoP / SiP 1 A Study of Underfill Property Optimization for 3D Package Board Level Reliability M.Amagai, H.Sano, Texas Instruments Japan / Japan 2 Development of Motion Control Module for Robots by SiP Technology T.Motomura, N.Morioka, K.Sasaoka, S.Sagara, O.Shimada, Dai Nippon Printing / Japan 3 Package on Package Design Optimization T.Hisada, J.Asai, R.Graf, IBM Japan / Japan 4 Thin Film Interposer Embedded Decoupling Capacitors for System in Package Applications T.Shioga, Y.Ishizuki, M.Mizukoshi, J.D.Baniecki, K.Kurihara, Fujitsu Laboratories / Japan 5 Post Encapsulation Grinding for MPS-C2 Ultra Thin Flip Chip Technology Y.Orii, K.Toriyama, Y.Oyama, T.Nishio, IBM Japan /Japan	[11C1] Materials & Processing I 1 Athermal Organic-Inorganic Nano Hybrid Material for Optical Waveguide Y.Shinba, Y.Tatsuta, N.Asahi, T.Nonaka, Toray Industories / Japan 2 Liquid Compression Mold for Package on Package (PoP) Y.Takahashi, M.Yoshino, K.Takano, Y.Chayama, K.Hayata, T.Onogami, K.Aoya, Texas Instruments / Japan 3 Technologies for Applying Fluids in Semiconductor Packaging A.J.Babiarz, Asymtek / USA 4 Transfer Method Using High-dielectric Film onto the Polymer Substrate M.Ichiki, University of Tokyo, JST-CREST, H.Furue, R.Maeda, National Institute of Advanced Industrial Science and Technology / Japan 5 Via-hole Formation by Excimer Laser and Their Via-hole Filling by Using Electro-plating T.Suzuki, T.Tamura, A.Fujisaki, R.Yaegashi, T.Urashima, T.Yamada, Noge Electric Industries, I.Koiwa, Kanto Gakuin University / Japan
11:05			
11:15	[11A2] Simulation II 1 Material Modeling of Interposer Card for Package-on-Package M.Kuzuno, H.Noma, T.Nishio, IBM Japan / Japan 2 Modeling of Power Distribution Network for Semiconductor Package using Organic Substrate M.Ishii, Y.Yamaji, S.Nakamura, T.Nishida, IBM Japan / Japan 3 The Impact of Probability in Yield Optimization on Wave Soldering Processes Y.Wikström, M.Ohvo, Turku University of Applied Sciences, A.Tuominen, University of Turku / Finland	[11B2] Environment/Lead Free 1 Ni Underlayer Efficiency Investigation for Whisker Mitigation in IC Packaging J.C.B.Lee, IST-Integrated Service Technology / Taiwan 2 Joining Technique for High Temperature Lead-Free Solder with Vacuum Evaporation Deposition T.Takahashi, T.Kono, Toshiba, S.Komatsu, Toshiba Research Consulting / Japan 3 Health Monitoring, Diagnostics and Prognostics of Electronic Products M. Pecht, University of Maryland / USA	[11C2] Materials & Processing II 1 Development of Nanocomposite Powder for Application of Resin Filler K.Hidaka, Hitachi / Japan 2 Innovative Processing Technologies for Wafer Thinning Process - Plasma Stress Relief Technology and Plasma Dicing Technology - K.Arita, Panasonic Factory Solutions / USA
12:30			
12:30 13:30	Lunch Time		
13:30	[11A3] High Frequency & RF & EMC I 1 Determination of Grounding Location for Guard Trace to Reduce Common-mode Radiation T.Matsushima, Y.Toyota, K.Iokibe, R.Koga, Okayama University, T.Watanabe, Industrial Technology Center of Okayama Prefecture, O.Wada, Kyoto University / Japan 2 A Novel Simply Model of Roughness Induced Power Consumption for GHz Propagation on Printed Circuit Boards H.Imai, A.Teramoto, S.Sugawa, T.Ohmi, Tohoku University, M.Sugimura, M.Kawasaki, Zeon / Japan 3 A Broadband Transition from a Via Structure to a Planar Transmission Line in a High-Speed Multilayer Board T.Kushta, T.Harada, NEC / Japan 4 Time Skew Control Methodology for High Speed Application Substrate Design P-H.Chang, B.Hsieh, K.Chiang, J-Y.Lai, Y-P.Wang, Siliconware Precision Industries / Taiwan	[11B3] Reliability I 1 Minimizing Solder Voids to Improve the BGA Solder Joint Drop Reliability Y.Y.Wang, Institute of High Performance Computing, T.Y.Lin, Motorola Innovation Centre / Singapore 2 The Effect of Electro-plated Cu Layer on Reliability of Solder Bump S.H.Lee, J.H.Kim, M.S.Suh, Q.H.Chung, K.Y.Byun, Hynix Semiconductor / Korea 3 Mechanical Effects of Driver Thickness on COG Connection with Non-conductive Adhesive P.Y.Tang, W-H.Sun, Hannstar Dispaly / Taiwan 4 Hermeticity and Thermal Stability Testing of PECVD Silicon Nitride Thin-film Packages Q.Li, Materials Innovation Institute, Delft University of Technology, NXP Semiconductor, J.F.L.Goosen, Delft University of Technology, J.T.M.Beek, NXP Semiconductor, F.Keulen, Delft University of Technology, K.L.Phan, B.Velzen, J.J.M.Bontemps, J.J.Koning, NXP Semiconductor, G.Q.Zhang, Delft University of Technology, NXP Semiconductor / The Netherlands	[11C3] Interconnection I 1 A Novel Process for Fabricating Ultra-High Coplanarity in Electroplating Lead-Free Copper Pillar Bump H-J.Hsu, J-T.Huang, P-S.Chao, S-H.Shih, National Taipei University of Technology / Taiwan 2 Observation of Bonded Area of Au Bump and Cu Lead with Sn Plating by Thermo-Compression Bonding M.Sogawa, F.Otsubo, T.Yamaguchi, H.Era, K.Nishio, Kyushu Institute of Technology / Japan 3 Development of a Novel JISSO Technique Using Laminating Process Y.Yanase, M.Nakasato, K.Saito, Y.Okayama, R.Usui, Y.Inoue, Sanyo Electric / Japan 4 Hydrogen Radical Reflow Characteristics of Small AuSn Solder Particles D.Chino, E.Higurashi, T.Suga, The University of Tokyo / Japan
15:10			
15:20	[11A4] High Frequency & RF & EMC II 1 EM Radiation from a Printed Circuit Board with an Interconnection Cable Driven by Low-Voltage Differential-Signaling Y.Kayano, Y.Ono, H.Inoue, Akita University / Japan 2 Effect of Package Common-Mode Current on PCB Power Bus Noise and Radiation U.Paoletti, T.Hisakado, O.Wada, Kyoto University / Japan 3 Research of Type Electromagnetic Wave Absorption Wall for RF-ID S.Sakaki, Y.Okano, Musashi Institute of Technology / Japan 4 Influence of Water Absorption on Dielectric Properties of Flexible Insulations K.Fukunaga, National Institute of Information and Communications Technology, S.Kurahashi, Industrial Research Center of Ehime / Japan	[11B4] Reliability II 1 Drop Test Reliability of Fine Pitch CSPs on Thin Multilayer Printed Wiring Board K.Fujii, K.Abe, Y.Oshima, T.Kitagawa, T.Ogatsu, NEC / Japan 2 Electrical and Thermal Characteristics of PCB with Embedded Active Device by Simultaneous Laminate Technology M.Tanaka, S.Amakai, S.Sagara, Dai Nippon Printing / Japan 3 Kirkendall Void Formation in Sn-3.5Ag/Cu Solder Joint J.Y.Kim, J.Yu, KAIST / Korea 4 Impact of Chip Package Interaction on Mechanical Reliability of Cu/ultra Low-k Interconnects in Flip Chip Package C.J.Uchibori, Fujitsu Labs. America, X.Zhang, P.S.Ho, University of Texas at Austin, T.Nakamura, Fujitsu Laboratories / USA, Japan	[11C4] Interconnection II 1 Effect of Ni Barrer Thikness at the Au-Sn Interface J.Y.Park, Korea Electronics Technology Institute / Korea 2 High Reliable Resin Core Bump Technology for 20μm pitch COG(Chip on Glass) Interconnection S.Tanaka, H.Imai, H.Ito, S.Mizuno, N.Hashimoto, A.Makabe, Seiko Epson / Japan 3 Connection Method between Flexible Printed Circuit and Indium Thin Oxide Electrode by Using Non-Conductive Film and Plating I.Koiwa, Y.Wakuda, Kanto Gakuin University, Y.Okura, K.Kawate, H.Yasui, Sumitomo 3M, H.Honma, Kanto Gakuin University / Japan 4 Flip Chip with B-stageable Polymer Bump and Pre-applied Underfill for RFID Applications B.Watanabe, D.Miyachika, Ablestik Japan, M.Mizukoshi, Fujitsu Laboratories / Japan
16:55			

June 12

	Room A	Room B	Room C
9:00	(9:25) [12A1] MEMS & Sensor I 1 Through Silicon Via for MEMS Packaging and Photo Sensors S.Denda, Nagano Prefectural Institute of Technology / Japan 2 Through-Hole Interconnection Formed by Femtosecond Laser Irradiation/Wet Etching and Molten Metal Suction Method for MEMS Package O.Nukaga, T.Suemasu, S.Yamamoto, H.Wakioka, H.Hashimoto, Fujikura / Japan 3 Development of High-precision Bonding Technology of Micro-components Using Manipulator and Laser Spot Heating for High-performance MEMS H.Motohara, M.Nakamura, Y.Kondoh, OLYMPUS / Japan 4 Novel Packaging Technology for Protecting Movable Parts with MEMS Devices M.Chino, N.Mayumi, T.Shimada, H.Tazawa, Misuzu Industries, T.Kamei, M.Yano, K.Machida, NTT Advanced Technology, N.Sato, K.Kuwabara, H.Ishii, NTT, E.Higurashi, The University of Tokyo / Japan	(9:25) [12B1] Liquid Device 1 A Portable Fuel Cell System for Portable Devices R.Jokinen, Turku University of Applied Sciences, A.Suominen, A.Tuominen, H.Lagercrantz, The University of Turku / Finland 2 The Polytetrafluoroethylene Processing Characteristics of High-energy(2keV-12keV) X-Ray and Its Application to Microfluidics Y. Ukita, University of Hyogo, Japan Society for the Promotion of Science, S.Yamamoto, Y.Utsumi, University of Hyogo / Japan 3 The Advanteges of Vertical Microreactor with Multifunctional Fluid Filter for Immunoassay Y. Ukita, University of Hyogo, Japan Society for the Promotion of Science, T.Omukai, S.Kondo, Y.Utsumi, University of Hyogo / Japan 4 Micro Fluid Device of PMMA for DNA Sequence by Using LIGA Process and Fusion Bonding D.Fukuoka, Y.Utsumi, University of Hyogo / Japan	[12C1] Substrate / Interposer 1 Flex to Board Interconnection with Non Conductive Thermosetting Adhesive K.Kawate, Y.Sato, S.Takeuchi, Sumitomo 3M / Japan 2 A Forming Method of Flat Fine Conductor on LTCC Green Sheet Using a Photo Resist Film Y.Akagi, J.Tane, N.Ota, Y.Yumisashi, F.Uchikoba, Nihon University / Japan 3 Development of New Alumina Substrate for High Power Devices M.Komura, M.Izumi, H.Arikawa, T.Hasegawa, Kyocera / Japan 4 COF Bonding Technology Using Tin Bumps and Non-conductive Adhesives (NCAs) for CMOS Image Sensor Device K-M.Harr, Y-H.Kim, Hanyang University, C-B.Lee, J-G.Kim, S.Yi, Samsung Electro-Mechanics / Korea 5 μPILR™ Technology for Advanced Mobile Packag Applications C.Ryu, K.Endo, C.Wade, Y.Kubota, I.Mohammed, V.Oganesian, Tessera / USA, Japan
11:05			
11:15	[12A2] MEMS & Sensor II 1 Innovative Application of MEMS-Based Method to Fabricate Pogo Pin Connector K-Y.Lee, J-T.Huang, H-J.Hsu, C-S.Wu, R-G.Wu, National Taipei University of Technology, M-Z.Lin, F-Y,Lee, C.C.P.Contact Probes / Taiwan 2 The Integration of CMOS Process Compatible Force Sensor and Scanning Signal Process Circuit for Vertical Probe Card J-T.Huang, K-Y.Lee, M-C.Chiu, H-J.Hsu, S-H.Shin, National Taipei University of Technology / Taiwan 3 Application of CMOS Dual-band RF Power Amplifier with On-chip MEMS Switch for Wireless Sensor Network J-T.Huang, S-H.Hung, H-J.Hsu, C-Y.Liu, National Taipei University of Technology / Taiwan	[12B2] Optoelectronics I 1 Surface-mount Packaging of VCSEL onto Single-mode Waveguide for High-density Optical Interconnects Board C.Ito, T.Komura, K.Nishio, Y.Awatsuji, S.Ura, Kyoto Institute of Technology / Japan 2 Proposal and Fabrication of New Cubic Optical Module for Optical Interconnect T.Ogawa, M.Kanda, O.Mikami, Tokai University / Japan 3 Free-space-waves Drop Demultiplexers Using Vertical Y-branch Waveguides for Ultra-high-density Optical Interconnects Boards T.Kobayashi, T.Muranishi, K.Nishio, K.Shimizu, Y.Awatsuji, S.Ura, Kyoto Institute of Technology / Japan	[12C2] Test & Analysis I 1 Test Method for Detecting Open Leads of Low Voltage LSIs A.Ono, M.Takagi, Takuma National College of Technology, M.Ichimiya, H.Yotsuyanagi, M.Hashizume, The University of Tokushima / Japan 2 New Ideas for Accelerated Testing and Analysis J.Kankaanranta, A.Tuominen, University of Turku, O.Hämeenoja, Nokia / Finland 3 An Inexpensive RF Power Meter for Cellular Phone Testing in Production Environment M.Maaspuro, A.Tuominen, Unversity of Turku, K.Airikkala, J.Sippola, I.Monkare, L.Pykari, Nokia Mobile Phones / Finland
12:30			
12:30 13:30	Lunch Time		
13:30	[12A3] MEMS & Sensor III 1 A DC-Contact RF-MEMS T/R Switch with Low-actuation Voltage Fabricated by CMOS-MEMS Processes J-T.Huang, P-H.Lin, S-Y.Li, National Taipei University of Technology / Taiwan 2 A Study of Carbon Nanotube Field Transistor Sensor Compatible with CMOS Process J-T.Huang, C.C.Yang, P-H.Lin, C-H.Lee, National Taipei University of Technology / Taiwan 3 Development of Micro Air Turbine by Silicon Multi Layer Stacking Y.Omori, K.Yamamoto, F.Uchikoba, Nihon University / Japan	[12B3] Optoelectronics II 1 Optical Connection Rod with Dam using UV Curable Resin by Mask Transfer Method Y.Nakanishi, M.Kanda, O.Mikami, Tokai University, N.Kojima, The Furukawa Electric / Japan 2 Application of Tapered Self-Written Optical Funnel to Positional Tolerance Improvement for Optical Interconnect Y.Sugiura, O.Mikami, Tokai University / Japan 3 On-Chip Optical Interconnect Structure Using Micro Plating Bumps and Its Application to Optical Clock Distribution T.Shimizu, M.Kinoshita, T.Ueno, J.Fujikata, K.Furue, K.Nishi, K.Ohashi, MIRAI-Selete / Japan	[12C3] Test & Analysis II 1 Macro Model of Driver Circuits for EMI Simulation N.Oka, K.Iokibe, Y.Toyota, R.Koga, Okayama University / Japan 2 Defects Analysis of High Electron Mobility Transistors Using Scanning Electron and Laser Beams Induced Current (SELBIC) H.Sueyoshi, Fukuoka University / Japan
14:45			
14:55		[12B4] Optoelectronics III 1 A Simple Optical Fiber Splicing Technique using CO_2 Laser Irradiation for Board-level Optical Interconnections S. Koike, S.Asakawa, R.Nagase, NTT, M.Kobayashi, NTT Advanced Technology / Japan 2 Development of 1.3/1.49μm One Package Bi-directional Module H.Nakanishi, Sumitomo Electric Industries / Japan 3 Observation of Flip-chip Bonded LEDs Directly on Ceramic Packages by Non-destructive Inspection Method T.Fukui, S.Fujii, T.Miyachi, H.Sakuta, S.Kurai, T.Taguchi, Yamaguchi University / Japan 4 Development and Application of Large-scale Integrated Light-Emitting Diodes T.Miyachi, H.Sakuta, S.Kurai, T.Taguchi, Yamaguchi University / Japan	[12C4] 3D 1 Investigation of the Thermal Resistance of a Three-dimensional (3D) Chip Stack from the Thermal Resistance Measurement and Modeling of a Single-stacked-chip K.Matsumoto, K.Sakuma, F.Yamada Y.Taira, IBM Japan / Japan 2 3 Dimensional Circuit Formation on Interference Reflecting Nano Layered Film with Nano Metal Printing for Near Field Radio Communication T.Arakawa, N.Terada, Harima Chemicals, S.Osada, S.Yanai, Toray Industries, T.Hanawa, K.Hashizume, Nokia Japan / Japan 3 Electroplating Copper Filling for 3-D Packaging F.Kuriyama, A.Fukunaga, A.Owatari, N.Saito, M.Nagai, Ebara / Japan 4 Reliability Assessment on Lead-Free Interconnection of 3D Chip Stacking with Tungsten Through-Silicon-Via K.Sakuma, P.S.Andry, R.Horton, C.K.Tsang, K.Sueoka, Y.Orii, Y.Oyama, C.Patel, S.L.Wright, B.Dang, E.Sprogis, J.U.Knickerbocker, IBM / Japan, USA
16:30			

Contact:

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