Advanced Program

ICEP2009

International Conference on Electronics Packaging

April 14 (Tue) -16 (Thu), 2009

Kyoto International Conference Center, Kyoto, Japan

The International Conference on Electronics Packaging (ICEP), of 2009 will be held from April 14th to April 16th at the Kyoto Kokusaikaikan, (the Kyoto International Conference Center), in Kyoto, Japan.

University/Plant tours are planned to various places including RITSUMEIKAN University's Micro-system Center and SR Center, as well as the TORAY Engineering Co., Ltd., (Equipment), SONY Mobile Display Corporation (LTPS; Low-Temperature Poly-Silicon), OMRON Corporation Electronic Components Company Micro-devices (MEMS), and KYOCERA SLC Technologies Corporation (PWB). These tours are planned on April 17th and are free of charge. Because the number of participants is limited, advanced registration is required. (early registration will be given priority) Optional tours around Kyoto City are also available for a reasonable fee.

The main focus of the ICEP2009 is "Collaboration". The conference will focus on the collaboration between Science, Engineering and Technology as well as collaboration between other different technologies.

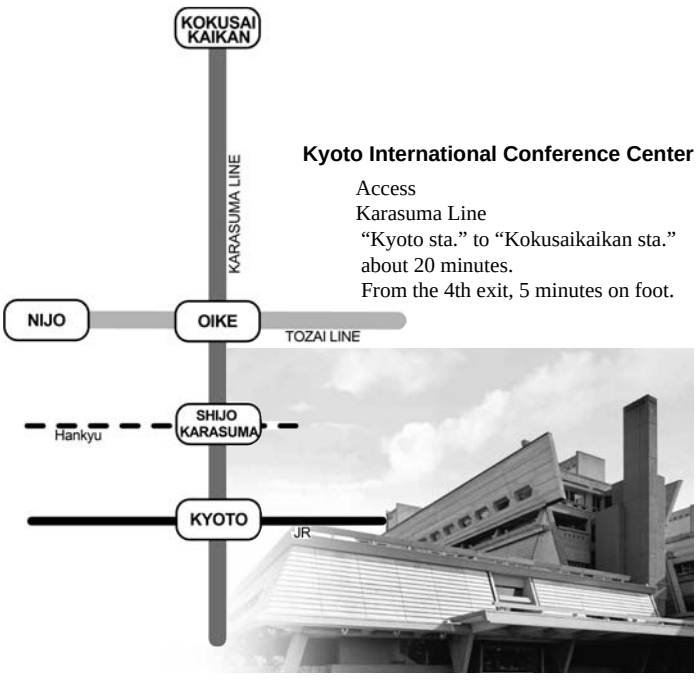
The conference's technical program will include three guest speakers and 45 technical sessions which include 17 core sessions that focus on recent trends and new areas of technology. The technical sessions include more than 170 technical papers regarding packaging technologies such as SiP/PoP, 3D packaging, and TSV/WLP, as well as Automotive Electronics concerns and information on Materials and Process issues. More than 20 student posters will also be presented. The conference promises to be a great event with something for everyone. Individuals who come to the conference will learn practical and profitable information and be able to participate in open discussions and face-to face communication.

We, the organization committee, are going to change the conference's focus to address what new paradigm shift is necessary in order to face current situations. We are looking forward to welcoming you to the conference.

"Join us and let's discuss JISSO together.", "Let's challenge for global solutions." and "Yes, we can!"

Hideyuki Nishida

ICEP2009 General Chairperson



Kyoto International Conference Center

Access
Karasuma Line
"Kyoto sta." to "Kokusaikaikan sta."
about 20 minutes.
From the 4th exit, 5 minutes on foot.

Sponsored by:
Japan Institute of Electronics Packaging (JIEP)
IEEE CPMT Society Japan Chapter

Contact:
Secretariat of ICEP 2009
JIEP,
3-12-2 Nishiogi-kita, Suginami-ku Tokyo 167-0042, Japan
http://www.jiep.or.jp/icep/

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Room A

(10:00)
[14A-1] High Performance Flip-Chip Packaging

1. Packaging Technologies for High Performance Computing System (Session Invite)
   J.Inasaka (NEC)/Japan
2. Spatial/Transient Thermal Resistance for High Performance FC Packages (Session Invite)
   K.Yazawa (SONY)/Japan
3. Facing Issues for Next Generation High Density Build Up Package Fabrication and the Alternative Solutions (Session Invite)
   S.Koyama (Shinko Electric Industries)/Japan
4. Power Integrity Optimization for a High-performance Microprocessor in Low-cost Systems
   S.Suminaga, H.Mori, T.Nishio (IBM Japan) /Japan

(11:40)

Lunch time

Poster Session

Room B1

(10:00)
[14B1-1] Embedded Substrate Ⅰ

1. WLP-IC Embedded Multi-layer Polyimide Wiring Board
   S.Okude (Fujikura)/Japan
2. Development of Embedded Passive / Active Devices Technology for Simultaneous Pressing Process
   H.Kamiya (DENSO)/Japan
3. IMB Technology for Embedded Active and Passive Components in SiP, SiB and Single IC Package Applications
   R.Tuominen, T.Waris, J.Mettovaara (Imbera Electronics)/Finland

[14B1-2] Embedded Substrate Ⅱ

1. Feasibility Study of Designing RF Band-pass Filters Using Embedded Passives Technique on Organic Substrate
   K.-C.Chin (Industrial Technology Research Institute)/Taiwan
2. Experimental Study of High Speed Transmission Performance of Substrate with Embedded Active Device
   M.Tanaka (Dai Nippon Printing)/Japan
3. Fabrication of Thin-Film Capacitors Using Aerosol CVD for High Performance Ceramic Package Applications
   S.Wang, A.Hattori, Y.Ozeki, W.Zhang, H.Ogawa (Noda Screen)/Japan

Lunch time

Poster Session

Room B2

(10:00)
[14B2-1] Optoelectronics Ⅰ

1. Adaptive Quad 10-Gbps Optical I/O Module for Power-Minimized Interconnection
   R.Kuribayashi, I.Hatakeyama, D.Inami, T.Hino, T.Sugimoto, K.Kurata (NEC)/Japan
2. Low-Loss, Chip-Based Optical Interconnects on Waveguide-Integrated SLC
   S.Nakagawa[1], H.Numata[1], Y.Taira[1], K.Kobayashi[2], K.Terada[2], M.Fukui[2] ([1]IBM, [2]Kyocera SLC Technologies)/Japan,
3. Embedded Micromirror Fabricated by Using Liquid Immersion Exposure for Thin Film Optical Interconnects
   K.Shimizu, T.Muranishi, J.Inoue, K.Nishio, K.Kintaka, Y.Awatsuji, S.Ura (Kyoto Institute of Technology)/Japan

[14B2-2] Optoelectronics Ⅱ

1. Multimode Polymer Optical Waveguide with Graded-Index Rectangular Cores for Optical Printed Circuit Broad
   T.Kosugi (Keio University)/Japan
2. Reflowable Surface Mount Optical Encoder
   J.Hane, Y.Kuroda, H.Fujita, T.Ito, I.Komazaki, E.Yamamoto (Olympus)/Japan
3. Reliability Improvement of Optical Devices by Using Newly Developed Highly Moisture Durable Optical Adhesives
   S.Mitachi (Tokyo University of Technology) /Japan

Lunch time

Poster Session

Room K

[14K-1] Energy / Environment

1. The IP Landscape for Photovoltaics
   C.E.Bauer, R.A.Fillion, H.J.Neuhaus (TechLead) /USA
2. Developing Direct Methanol Fuel Cell from Basic Research Results; Process View
   A.Suominen[1], R.Jokinen[2], M.Fonsell[2], A.Tuominen[1] ([1]University of Turku, [2]Turku University of Applied Sciences) /Finland
3. Developing Direct Methanol Fuel Cell from Basic Research Results; Technical Aspects
   R.Jokinen[2], A.Suominen[1], M.Fonsell[2], A.Tuominen[1], ([1]University of Turku, [2]Turku University of Applied Sciences)/Finland
4. Innovative Jisso Structure by Skeleton Circuit Structure
   H.Hayashi (The University of Tokyo) /Japan

(10:40)

(10:50)
[14K-2] Lead Free / Environment

1. Effect of Mn Addition on Properties of Sn-Ag-Cu-In Quaternary Lead-free Solder Alloy
   A.-M.Yu[1], J.-K.Kim[1], J.-H.Lee[2], M.-S.Kim[3] ([1]Korea Institute of Industrial Technology, [2]Seoul National University of Technology, [3]Inha University)/Korea
2. Inhibition of Cracking in Cu_6Sn_5 Intermetallic Compounds at Sn-Cu Lead-Free Solders and Cu Substrate Interfaces
   K.Nogita[1], S.Suenaga[2], S.D.McDonald[1], H.Tsukamoto[1], J.Read[1], T.Nishimura[2] ([1]The University of Queensland, [2]Nihon Superior) /Australia, Japan
3. Impact Strength of Sn-Cu (-Ni) Lead-Free Solder Ball Grid Arrays Placed on Cu Substrates
   H.Tsukamoto[1], T.Nishimura[2], S.Suenaga[2], S.D.McDonald[1], J.Read[1], K. Nogita[1] ([1]The University of Queensland, [2]Nihon Superior) /Australia, Japan
4. Microstructure and Mechnical Properties of Sn-Bi Eutectic Solder
   S.Sakuyama (Fujitsu Laboratories)/Japan

(12:30)

13:40 **Japanese Noh Drama**
(Room A)

13:55 – 14:25 **Welcome Ceremony & Awarding Ceremony ICEP2008**
(Room A)

14:25 – 17:35 **Invited Speeches**
(Room A)

1. Packaging Technology Roadmap - An IBM Perspective
   Peter Brofman (IBM)
2. Memory Packaging Strategy with Sophisticated Technology
   Takayuki Watanabe (Akita Elpida Memory)
3. Photovoltaic as An Energy Solution
   Tetsuroh Muramatsu (Sharp)

18:00 – 20:00 **Welcome Reception**
(Banquet Hall “Swan”)

Room A

09:00 **[15A-1] Advanced Packaging Ⅰ**

1. A Reliability Test on PBGA Packaging Through Piezoresistive Stress Sensor
   C.H.Liu[1], H.Chung[1], D.W.Yang[1], K.F.Tseng[2], B.J.Lwo[1] ([1]National Defense University, [2]Chin-Min Institute of Technology)/Taiwan
2. Evaluation of the Effect of Packaging Process Parameters on Semiconductor Devices with Low-k Conductive Layers
   T. Yamada[1], M.Masumoto[2], O.Horiuchi[1], H.Tomokage[2] ([1]Fukuoka Industry, Science & Technology Foundation, [2]Fukuoka University)/Japan
3. The Solder Blister Control for Lead Frame Packages
   J.W.Chen[1], S.Lee[1], B.Appelt[2], A.Tseng[2] ([1]Advanced Semiconductor Enginrrring, [2]ASE(US))/Taiwan, USA
4. First Generation of Stretchable No-Light Emitting Display Based on Stretchable Electronic Technologies for Textile Application
   A.Fabrice (IMEC)/Belgium

10:40

10:50 **[15A-2] Advanced Packaging Ⅱ**

1. Low-Temperature Wafer Bonding by Ar-Beam Surface Activation
   Y.-H.Wang, S.Taniyama, T.Suga (The University of Tokyo)/Japan
2. Wafer-to-Wafer Alignment Using Moire Pattern and its Interests for 3D Integration
   C.Wang, T.Suga (The University of Tokyo) /Japan
3. A Multilayer Process for 3D-Molded-Interconnect-Devices to Enable the Assembly of Area Array Based Package Types
   T.Leneke (Otto-von-Guericke University of Magdeburg)/Germany
4. 3D Packaging: up to 30 GHz for Integrated Antenna Front-Ends
   C.Drevon[1], B.Bonnet[1], P.Monfraix[1], R.Chiniard[1], C.Val[2], H.Legay[1], P.Couderc[2], J.-L.Cazaux[1] ([1]Thales Alenia Space, [2]3DPlus) /France

12:30

12:30 13:30 **Lunch time Poster Session**

Room B1

[15B1-1] Embedded Substrate Ⅲ

1. Novel Approach in Design and Test of Embedded Capacitors in Organic-based Substrate for Highly Compact RF Systems-in-Package Devices
   C.Romero, J.Lim, Y.H.Yoon, T.Kim, S.Yi (Samsung Electro Mechanics)/Korea
2. Electrodeposition of High-k Titania Thin Films for Embedded Capacitors
   B.K.Roy, J.Cho (State University of New York Binghamton)/USA
3. The Nanotransfer Technology of the PZT Capacitor for the Application of Embedded Substrate
   S.Makino, M.Ichiki, R.Maeda, T.Suga (The University of Tokyo, AIST, JST-CREST)/Japan

(10:15)

(10:25)

[15B1-2] LED

1. Refraction Index, Transmittance and Shape Dependence of Light Extraction from Near-ultraviolet Light-emitting Diode
   H.Hayashi (Yamaguchi University)/Japan
2. Luminous and Thermal Characteristics of High Power Near-ultraviolet LED Packages with Various Chip Arrangemants
   K.Kamon (Yamaguchi University)/Japan
3. Analysis of Thermal Performance for High Power Light Emitting Diodes Lighting Modulus
   W.-H.Chi, T.-L.Chou, C.-N.Han, S.-Y.Yang, K.N.Chiang (National Tsing Hua University) /Taiwan
4. Thick Film Pastes for the Manufacture of Low Cost, Insulated Aluminum Substrates for Use as Integrated Heat Sinks for High Intensity LEDs
   K.Takarabe (ESL Nippon)/Japan
5. The Behavior of Thermal and UV Degradiation between LED Encapsulation and their Devices
   C.-W.Hsu, C.-H.Lin, H.-T.Li, S.-C.Huang, K.-C.Chen (Industrial Technology Research Institute)/Taiwan

Lunch time Poster Session

13:30 **[15A-3] 3D/TSV Ⅰ**

1. Integration of Compliant Bump with Through-Si-Via Technology and Its Application Back-Side Illuminated CMOS Image Sensor(Session Invite)
   T.Asano[1], N.Watanabe[2], I.Tsunoda[2], Y.Takao[1], K.Tanaka[3], T.Higashimachi[4], Y.Yamaji[5], M.Aoyagi[5], T.Kyotani[6], H.Arao[7], Y.Kimiya[8], K.Fukunaga[8], A.Ikeda[1], Y.Kuroki[1], T.Tsurushima[1] ([1]Kyushu University, [2]Fukuoka Industry Science & Technology Foundation, [3]Kyushu Sangyo University, [4]Sojo University, [5]AIST, [6]PMT, [7]JGC Catalysts and Chemicals, [8]Yoshidama Surface Finishing) /Japan
2. 3D Packaging and Interconnect Technologies at CEA-Leti Minatec (Session Invite)
   M.Scannell (CEA-Leti)/France
3. TSV and Wafer Level Packaging Approaches to 3D Packaging
   E.J.Vardaman (TechSearch International)/USA
4. Thermal Characterization of a Three-dimensional (3D) Chip Stack
   K.Matsumoto, Y.Taira (IBM)/Japan
5. Bonding Strength Estimation of BCB Dielectric Film in 3D Stacked IC Packages
   M.-C.Hsieh, C.-Y. Cheng, W.Lee, R.-M. Tain (Industrial Technology Research Institute) /Taiwan

15:35

15:45 **[15A-4] 3D/TSV Ⅱ**

1. Inter Chip Fill for 3D Chip Stack
   A.Horibe, F.amada, J.Knickerbocker, C.Feger (IBM)/Japan
2. Die-cracking Evaluation of Silicon Chip Coverd with Polymer Film for 3D Chip Stacking Packages
   C.-J.Wu[1], M.C.Hsieh[2], K.N.Chiang[1] ([1]National Tsing-Hua Univercity, [2]Industrial Technology Research Institute)/Taiwan
3. Characterisation of Through Silicon Via (TSV) Processes Utilising Mass Metrology
   L.Cunnane, A.Kiermasz, G.Ditmer (Metryx) /UK

17:00

17:10 **[15A-5] 3D/TSV Ⅲ**

1. Cost Effective PVD Solution which Enable TSV Integration in the Emerging 3-D Market
   B.Ninan, A.Wang (Tango Systems)/UK
2. Delivering High Reliability from a Wafer-Scale, Chip-Sized Package Incorporating a Through Silicon Via Solution
   M.Kriman (Tessera)/Israel
3. Development of Interconnect Technology in 25 Micron Pitch for Low Cost CoC(Chip on Chip)
   T.Norimatsu (Fujitsu Microelectronics)/Japan

(18:25)

18:50

Lunch time Poster Session

[15B1-3] Printed Electronics Ⅰ

1. Printable Electronics on Flexible Substrate by Inkjet Technology (Session Invite)
   S.Nishi (Konicaminolta IJ Technologies)/Japan
2. Palm Top Sized Super Fine Inkjet System and Mask Less Direct Patterning (Session Invite)
   K.Murata, K.Shimizu (Advanced Industrial Science and Technology)/Japan
3. Electric Conductive Film Formations by Ink-jet using Individually Dispersed Nanoparticle Ink formed by Gas Evaporation Method (Session Invite)
   M.Oda (ULVAC)/Japan
4. Inkjet Printing of Silver Nanopaste for Printed Electronics (Session Invite)
   S.Abe (Harima Chemicals)/Japan
5. Silver and Copper Nanoparticles and Their Application to Wring Formation and Joining (Session Invite)
   M.Nakamoto (Osaka Municipal Technical Research Institute)/Japan

Lunch time Poster Session

[15B1-4] Printed Electronics Ⅱ

1. Advantages of Ink-Jet Printing in LTCC Production Technology (Session Invite)
   Y.Kawamura (KOA)/Japan
2. Embedded Passives with High Precision and Wide Range Build on Plastic Substrates
   M.Nakayama (NY Industries)/Japan
3. Advanced Fine Line Thick Film Conductors with High Conductivity and Solderability Build by Screen-printing
   D.K. Numakura (DKN Research)/USA

[15B1-5] Printed Electronics Ⅲ

1. Fabrication of RF Circuit Structures on a PCB Material by Inkjet Printing and Electroless Plating
   A.Sridhar[1], M.Perik[2], J.Reiding[2] ([1]University of Twente, [2]Saxion Hogeschool)/The Netherlands
2. Effects of Cold Crystallization on Morphology and Thermal Charctterstic of Poly (9, 9-di-n-octyl-2, 7-fluorene)(PFO)
   B.-Y.Su[1], H.C.Chen[1], C.L.Chung[1], S.L.Fu[1], C.-Y.Ou[2] ([1]I-Shou University, [2]Research Alliance Taiwan TFT LCD Assciation)/Taiwan
3. Pattering of ITO Microwire Using Laser-induced Thermal Printing Method
   S.Iwasaki[1], T.Sano[1], S.Katsura[2], K.Yoshida[3], A.Nakayama[4], A.Hirose[1] ([1]Osaka University, [2]Nippon Denki Kagaku, [3]General Technology, [4]Ion Technology Center)/Japan

(18:25)

Room B2

[15B2-1] Interconnections Ⅰ

1. Effect of the Formation of the Intermetallic Commpounds between a Tin Bump and an Electroplated Copper Thin Film on Both Mechanical and Electrical Properties of the Jointed Structures
   S.Jeong, K.Suzuki, H.Miura (Tohoku University) /Japan
2. Comparison of Thermal Fatigue Life of SAC Solder Joints and SnPb Solder Joints with Various Stress Ranges
   S.W.R.Lee, C.Yang, Y.S.Chan (Hong Kong University of Science and Technology)/Hong Kong
3. Thermomigration in Eutectic SnPb Solder Joint
   Y.Tao[1], Q.Cheng[1], G,-R.Tang[1], B.Wang[1], B.An[1], F.-S.Wu[1], Y.-P.Wu[1,2] ([1]Huazhong University of Science and Technology, [2]Wuhan National Laboratory for Optoelectronics)/China
4. Concave Shape in Gold-Solder Interconnection System
   J.-Y.Park, E.-J.Choi, S.-C.Lee, Y.-B.Sun (Kyonggi University)/Korea

[15B2-2] Interconnections Ⅱ

1. Development of Ultrasonic Flip-Chip Bonding Interconnection Technologies for COB Modules
   K.Marusaki (Sharp)/Japan
2. Chip-on Flex(COF) Bonding Technology Using Tin Bumps and Non-Conductive Adhesives (NCAs) for CMOS Image Sensor Device
   K.-M.Harr[1], D.-H.Kim[1], Y.-M.kim[1], H.-Y.Cho[1], C.-B.Lee[2], J.-G.Kim[2], S.Yi[2], Y.-H.kim[1] ([1]Hanyang University, [2]Samsung Electro-Mechnics)/Korea
3. Evaluating the Performance of Thermosetting Resins under Ultrasonic Bonding Process
   S.H.Huang[1], H.C.Chen[1], C.L.Chung[1], S.L.Fu[1], S.C.Ho[2], A.H.Liu[2], Y.J.Lee[2] ([1]I-Shou University, [2]ChipMOS Technologies)/Taiwan
4. An Anisotropic Conductive Adhesive Improved by Carbon Nanotubes and Its Application on RFID Tag Inlays Packaging
   X.-H.Cai[1], B.An[1], F.-S.Wu[1], Y.-P.Wu[1,2] ([1]Huazhong University of Science and Technology, [2]Wuhan National Laboratory for Optoelectronics)/China

Lunch time Poster Session

[15B2-3] Interconnections Ⅲ

1. The Semi-experiment Analysis of the Wire Sweep of a Wire Bond during the Transfer Molding Process
   H.-K.Kung[1], H.-S.Chen[1], H.-C.Hsu[2] ([1]Cheng Shiu University, [2]I-Shou University)/Taiwan
2. Micro-bumping Technology by PPS Method
   K.Tsuruta (Senju Metal Industry)/Japan
3. Flip Chip Assembly on 50-um-pitch Pads Soldered with Precoat by Powder Sheet
   H.Noma (IBM Japan)/Japan
4. Investigation on Wet-Chemical Surface-Cleaning of Au Bump for Low-Temperature Chip Stack-Bonding Using Compliant Bump
   T.Mori[1], N.Watanabe[2], T.Asano[1]([1]Kyushu University, [2]Fukuoka Industry Science & Technology Foundation)/Japan
5. Formation of Micro Au Bump Array for Flip-Chip Bonding using Electroless Au Deposition
   T.Yokosima[1], K.Nomura[1,2], Y.Yamaji[1], K.Kikuchi[1], H.Nakagawa[1], K.Koshiji[1], M.Aoyagi[1,2], R.Iwai[3], T.Tokuhisa[3], M.Kato[3] ([1]National Institute of Advanced Industrial Science and Technology, [2]Tokyo University of Science, [3]Kanto Chemical)/Japan

[15B2-4] Interconnections Ⅳ

1. Room Temperature Sintering and Bonding with Ag Nanoparticle Paste
   D.Wakuda, K.-S.Kim, K.Suganuma (Osaka University)/Japan
2. Fablication of Large-scale Nanoparticle Array using Combination of Self-assembly and 2-step Transfer
   K.Sugano, T.Ozaki, R.Hiraoka, T.Tsuchiya, O.Tabata (Kyoto University)/Japan
3. Direct Bonding to Aluminum Utilizing Silver-oxide Particles
   Y.Yasuda, E.Ide, T.Morita (Hitachi)/Japan

[15B2-5] Interconnections Ⅴ

1. Quantitative Measurement of Air-gap of Silicon/Silicon Interfaces
   M.M.R.Howlader, M.G.Kibria, F.Zhang, T. Suga (McMaster University)/Canada
2. Evalution of Electric Contact Phenomena under Small Contact Load
   O.Mukhtar (Osaka University)/Japan
3. True 3D Through Hole Interconnections
   H.Wakioka (Fujikura)/Japan
4. Open Lead Detection Circuit for QFP ICs Using Logic Gates as Open Sensors
   M.Hashizume (University of Tokushima)/Japan

Room K

[15K-1] Electrical Solutions Ⅰ

1. Effects of Uni-axial Mechanical Stress on the Scattering Parameters of Metal-oxide-semiconductor Field Effect Transistors
   Y.Han[1], M.Koganemaru[2], T.Ikeda[3], N.Miyazaki[3], Y.Kiyotaka[4], W.Choi[4], H.Tomokage[4] ([1]Fukuoka Industry Science & Technology Foundation, [2]Fukuoka Industrial Technology Center, [3]Kyoto University, [4]Fukuoka University)/Japan
2. Bandwidth Simulation for High Speed Memory
   C.-P.Chen, J.-H.Cheng, W.-J.Fan, N.-C.Lin, T.-F.Su (Powertech Technology)/Taiwan
3. Preliminary Study and Design of CMOS Diode for Electrostatic Discharge Protection
   N.F.Muhammad, A.Ibrahim, A.R.Ahmad, M.R.Yahya (Telekom Research & Development) /Malaysia
4. Electrical Characterization of Micro Spring Probe Card for Wafer Level Testing
   H.-Y. Chang (Advanced Semiconductor Engineering)/Taiwan
5. A Target Impedance Profile of Power Distribution System Considering On-Chip Model
   N.Takahashi[1], K.Kagawa[2], K.Hoshino[3] ([1]IBM Japan, [2]ATE Service, [3]Shibaura Institute of Technology)/Japan

(11:05)

(11:15)

[15K-2] Electrical Solutions Ⅱ

1. The Possibility of JISO using Micro Contact
   S.Yoshida, S.Murata, K.Soeta (ALPS Electric)/Japan
2. High-speed Intra-Body Transmission System Using 2 - 28 MHz OFDM Modulation
   F.Koshiji, S.Takenaka, K.Sasaki (The University of Tokyo)/Japan
3. RFID and its Applications in Tourism
   T.Hu (Aizu University)/Japan

[15K-3] Mechanical Solutions

1. Measurement of Three-dimensional Surface Displacement Using the Digital Image Correlation with AFM Images
   N.Shishido, T.Ikeda, N.Miyazaki (Kyoto University)/Japan
2. Multi-angle View Visual Inspection of Solder Joints with Neural Networks
   M.Matsushima (Osaka University)/Japan
3. Package Warpage Simulation Using FEM Visco-Elastic and Cure Degree Coupling
   I.Hirata (NEC)/Japan
4. Numerical Simulation of Variable Frequency Microwave Curing of Underfill Materials
   T.Tilford[1], K.I.Sinclair[2], C.Bailey[1], M.P.Y.Desmulliez[2] ([1]University of Greenwich, [2]Heriot-Watt University)/UK
5. Substrate Trapezoidal Trace Shape Modeling
   L.C.Kim, B.J.Kai (Intel Microelectronic)/Malaysia

[15K-4] Thermal Management Ⅰ

1. Thermal Design of RGB LED Modules
   A.Andonova, N.Kafadarova (Technical University Sofia)/Bulgaria
2. Comprehensive Thermomechanical Lifetime Calculation of a Soldered Assembly
   G.Massiot, M.Grieu, O.Maire, C.Munier (EADS France)/France
3. Experimental Simulative Analysis for Thermal Performances of Vertical Stacked Die Packages
   C.-K.Yu, C.-K.Liu, S.-L.Kuo, M.-J.Dai, Y.-L.Chao, C.-Y.Hsu, R.-M.Tain (Industrial Technology Research Institute)/Taiwan

[15K-5] Thermal Management Ⅱ

1. Radiation Cooling Effects on LSI Chip Temerpature with an Alumina Heat Sink of High Infrated Emmisivity Material
   K.Shinagawa[1], M.Nishimura[2], S.Hirokawa[1], Y.Muto[1] ([1]Canon Marketing Japan, [2]NISHIMURA PORCLEAN)/Japan
2. Emissivity Stability Investigation of Substrates and Layers in Microelectronics
   V.Videkov, A.Andonova, N.Kafadarova (Technical University Sofia)/Bulgaria
3. Precursor Monitoring Approach for Reliability Assessment of Cooling Fans
   T.Shibutani[1], H.Oh[2], M.Pecht[2] ([1]Yokohama National University, [2]University of Maryland)/Japan, USA
4. Design and Optimization of 3D Manifold of Microchannel Heat Sink using the Porous Media Approach
   L.F.Yau (Nationa University of Malaysia) /Malaysia

Room A

09:00

[16A-1] SiP/PoP Advanced Assembly Ⅰ

1. PoP Technology for Mobile Phone Manufacturing – Past, Present and Future (Session Invite)
   Y.Wada (Nokia Japan)/Japan
2. 3D Technology Roadmap and the Global Competition (Session Invite)
   H.Nakajima (NEC Electronics)/Japan
3. Flip Chip SiP and Advances (Session Invite)
   H.Shimamoto (Renessas)/Japan
4. (Session Invite)
   A New Novel Dual Face Package
   M.Ishihara (Kyushu Institure of Technology) /Japan

10:40

10:50

[16A-2] SiP/PoP Advanced Assembly Ⅱ

1. Gold Stud Bumps for Hight Performance Flip Chip Packages
   W.Chen[1], K.Shen[1], A.Wang[1], Y.Lai[1], B.Appelt[2], A.Tseng[2] ([1]Advanced Semiconductor Enginrrring, [2]ASE(US))/Taiwan, USA
2. Novel Compact Connector for PoP and BoB Applications
   K.-S.Choi[1], H.-C.Bae[1], D.-S.Jun[1], J.-T.Moon[1], K.-B.Cha[2], D.-Y.Kim[2], Y.-I.Jun[1] ([1]Electonics and Telecommnucations Resarch Institute, [2]Unisemicon)/Korea
3. Wettability and Reliability on Double Side Assembly with MPS-C2 Flip Chip Technology
   H.Noma, Y.Oyama, H.Nishiwaki, M.Takami, T.Takatani, K.Toriyama, Y.Orii (IBM Japan) /Japan
4. Effect of Packaging Process Parameters on the Damage of Semiconductor Device with Low-k Materials
   M.Masumoto[1], O.Horiuchi[2], T.Yamada[2], J.Morishita[3], W.Choi[4], H.Tomokage[4] ([1]Texas Instruments, [2]Fukuoka Industry, Science & Technology Foundation, [3]Walts, [4]Fukuoka University)/Japan

12:30

12:30 / 13:30

Lunch time
Poster Session

13:30

[16A-3] Fine MEMS Ⅰ

1. Nano-mechanical Structure Fabrication Technology for Highly Integrated, Complex MEMS (Tentative) (Session Invite)
   I. Shimoyama (The University of Tokyo)/Japan (Tentative)
2. High Density Integration Technology with Laser Assisted Inkjet Writing (Session Invite)
   J.Akedo (National Institute of Advanced Industrial Science and Technology)/Japan
3. Highly Integrated MEMS-Pseudo-SOC Technology (Session Invite)
   H.Yamada (Toshiba)/Japan

(14:45)

(14:55)

[16A-4] Fine MEMS Ⅱ

1. High Density Packaging Technology Using Low Temperature Chip Stacking for Fine-MEMS (Tentative) (Session Invite)
   M.Koyanagi, T.Fukushima, T.Tanaka (Tohoku University)/Japan (Tentative)

15:10

15:20

2. Mass-production Technology for Vertical Integrated MEMS (Session Invite)
   S.Lee (OMRON)/Japan
3. Wafer-Level Bonding Technology for Different Materials (Session Invite)
   E.Shimizu, T.Suyama, R.Ohta (Olympus)/Japan

(16:10)

(16:20)

[16A-5] Assembly Technology for MEMS

1. A Novel Microfabricated Fibrillar Structure Inspired from Biological Attachment Systems
   H.Parsaiyan, F.Barazandeh, S.M.Rezaei, M.S.Hajhashem (Amirkabir University of Technology)/Iran
2. Parylene Embedded Metal Interconnects for Stretchable Silicon Electronics
   T.Zoumpoulidis[1], M.Bartek[1], R.Dekker[1,2] ([1]Delft University of Technology, [2]Philips Research)/The Netherlands
3. Laser Assisted Ink Jet Printing for Fine Ag Wiring
   A.Endo, J.Akedo (National Institute of Advanced Industrial Science and Technology)/Japan
4. Development of Wafer Level CSP for Micro Electro Mechanical Systems
   H.Tenmei[1], K.Matsumoto[2], M.Nakajima[2], M.Sugita[2], S.Nagashima[2] ([1]Hitachi, [2]Hitachi Media Electronics)/Japan
5. Low Temperature Wafer Bonding using Metal Diffusion Technique
   H.Kurotaki[1], H.Shinohara[2], H.Kobayashi[1], J.Mizuno[2], S.Shoji[2] ([1]EV Group Japan, [2]Waseda University)/Japan

(18:25)

18:50

Room B1

[16B1-1] Material Ⅰ

1. Low-temperature Curable and Electrically Conductive Paste for Touch Panels and LCD Panels
   J.Bai, R.Chu, S.Gupta (Henkel Japan)/Japan
2. The Effect of Conductive Particle Parameters on Electronical Conductvity in Anisotropic Conductive Film Joints
   J.-H.Kuang, C.-M.Hsu (National Sun Yat-Sen Universtity)/Taiwan
3. Study of the Filler Effect on the Effective Thermal Conductivity of Thermal Conductive Adhesive
   Y.Zhang[1], C.Yue[1], J.Liu[1,2], Z.Cheng[2], J.-Y.Fan[1] ([1]Shanghai University, [2]Chalmers University of Technology)/China, Sweden
4. Thermal Conductivity of Electrically Conductive Adhesives Containing Fillers with Multi-modal Paricle Size Distibutions
   M.Inoue[1], J.Liu[2,3] ([1]Osaka University, [2]Chalmers University of Technology, [3]Shanghai University) /Japan, Sweden, China

[16B1-2] MEMS / TSV Key Technologies

1. Micropump with Cross-junction Channels for Application in Gas Rate Sensor
   V.T.Dau, K.Tanaka, S.Sugiyama (Ritsumeikan University)/Japan
2. An Investigation into Deep RIE-based Through-Si-Via(TSV) Microfabrication for 3-D System-in-package(SiP) Integration
   M.Miao[1,2], Y.Jin[1], H.Liao[1], L.Zhao[1], Y.Zhu[1], X.Sun[1] ([1]Peking University, [2]Beijing Information Science and Technology University)/China
3. Cu Fill Properties in the High Aspect Ratio Through Si Via Hole by Electroless Plating
   F.Inoue[1], K.Yamamoto[2], S.Tanaka[2], Z.Wang[3], S.Shingubara[1] ([1]Kansai Uninersity, [2]National Institute of Communication Technology, [3]Shaanxi Normal University)/Japan, China
4. Electrohydrodynamic Micropumps for Electronic Chip Cooling Applications (Session Invite)
   P.R.Selvaganapathy, C.Y.Ching(McMaster University)/Canada

Lunch time
Poster Session

[16B1-3] Automotive Electronics, Future Requirements

1. Launch-up of Adopting BGA into Engine ECU in Japan (Session Invite)
   H.Ueda (SemiConsult)/Japan
2. Development of IGBT Power Module with Anodized Metal Substrate (AMS) for Hybrid Electric Vehicle (HEV) Application (Session Invite)
   S.Gao, J.Kim, D.Yoo, S.Choi, S.Yi (Samsung Electro-Mechanics)/Korea
3. Design Concepts of New Components for Next Generation Automotive Power Electronics (Session Invite)
   T.Tominaga (CalsonicKansei)/Japan
4. Ink Jet Marking on Bare Die for Chip Traceability (Session Invite)
   H.Kawaguchi (Toray Engineering)/Japan

[16B1-4] Automotive Electronics, Challenges

1. Thermal Management of LED Headlamp System (Session Invite)
   S.Gao, S.Shin, Y.Lee, J.Kim, S.Choi, S.Yi (Samsung Electro-Mechanics)/Korea
2. Pb-free High Temperature Solder Joints for Power Semiconductor Device (Session Invite)
   Y.Yamada[1], Y.Takaku[2], Y.Yagi[1], I.Nakagawa[3], T.Atsumi[3], M.Shirai[3], I.Ohnuma[4], K.Ishida[4] ([1]Toyota Central Research & Development Laboratories, [2]Tohoku University CREST-JST, [3]Toyota Motor, [4]Tohoku University)/Japan
3. High Relaibility Solder for Car Electronics (Session Invite)
   M.Ueshima (Senju Metal Industry)/Japan
4. Drop Impact Reliability and Thermal Cycle Resistivity of Low-Ag Content Sn-Ag-Cu Solders (Session Invite)
   T.Sasaki (Nippon Steel)/Japan

(17:00)

(17:10)

[16B1-5] Electrical Solutions Ⅲ

1. Novel Highly-Integrated Common-Mode Resonant Filters Based on Multilayer Board Technologies
   T.Kushta (NEC)/Japan
2. Bond Pass Filter Embedded System with Probe (SwP) for High Frequency Application
   K.Matsumoto, R.Saito, W.Choi, H.Tomokage (Fukuoka University)/Japan
3. Reduction of EMI from Differential Signaling System Using Asymmetry Guard Trace
   T.Matsushima[1], Y.Toyota[1], K.Iokibe[1], R.Koga[1], T.Watanabe[2], O.Wada[3] ([1]Okayama University, [2]Industrial Technology Center of Okayama Prefecture, [3]Kyoto University)/Japan
4. Prediction of EM Radiation from a Printed Circuit Board Driven by Differential-Signaling
   Y.Kayano, H.Inoue (Akita University)/Japan

Room B2

[16B2-1] MFG/Process Ⅰ

1. Design of Experiment (DOE) Study for the Optimization of Lapping Process of GaAs Wafer for Wireless Device Application
   N.H.Ghazali, N.A.Omar, N.A.Ngah, A.Dolah, M.R.Yahya (Telekom Research & Development) /Malaysia
2. A Forming Method of Cavity Structure with LTCC Substrate Using Photo Resist Film
   Y.Akagi (Nihon University)/Japan
3. Inductive Modeling of Laser Trimming of Film Resistors
   J.Autonov (The Ulyanovsk State Technical University)/Russia
4. Influence of Deformation of Single Crystalline Copper on its Surface Activated Bonding at Room Temperature
   R.Takagishi, M.Akaike, T.Suga (The University of Tokyo)/Japan

[16B2-2] MFG/Process Ⅱ

1. Studies on Low-temperature Direct Bonding Methods of PMMA and COP Using Surface Pretreatment
   H.Shinohara, J.Mizuno, S.Shoji (Waseda University)/Japan
2. High Reliability Encapsulant Liquid Resin for SIP - The Simultaneous Process of over Mold and Underfill by VPES(Vacuum Printing Encapsulation Systems)
   K.Nagai, Y.Ishikawa, A.Okuno (SANYU REC) /Japan
3. A Novel Metal-to-metal Bonding Process Utilizing Low-temperature Sinterability of Ag_2O^- derived Ag Nanoparticles
   N.Takeda[1], H.Tatsumi[1], Y.Akada[1], T.Ogura *[1], E.Ide[2], T.Morita[2], A.Hirose[1] ([1]Osaka University,[2] Hitachi)/Japan
4. Assembly Technique of 0402size Chip on Flexible Printed Circuits
   T.Kitada (Fujikura)/Japan.

Lunch time
Poster Session

[16B2-3] MFG/Process Ⅲ

1. Die Product Assembly on Flex Substrate
   T.Onishi (Grand Joint Technology)/Hong Kong
2. Investigation of Flip Chip Bonding with NCF
   N.Asahi, K.Fujimaru, T.Nishiyama, K.Kasumi, K.Matsumura, T.Nonaka (Toray Industries) /Japan
3. Flip Chip Bonding with Elasticity Bonding System (EBS) Method
   R.Kojima (Sony Chemical & Information Device) /Japan
4. Effect of the Excimer Irradiation Process on the Interconnection of Flip Chip Bonding
   K.Sakuma[1,2], N.Nagai[1], J.Mizuno[1], S.Shoji[1] ([1]Waseda University, [2]IBM)/Japan

[16B2-4] Substrate Ⅰ

1. Microstructural and Dielectric Characterization of Alumina-Based LTCC Materials
   A.Ibrahim[1], R.Alias[1], M.H.A.R.M.Ahmad[2], C.S.Mahmood[2], M.R.Yahya[1], A.F.A.Mat[1] ([1]Telekom Research & Development, [2]MTEC) /Malaysia
2. Thermal Conductivity Characterization of Al_2O_3-SiO_2-PbO-MgO Tape System for High Frequency Substrate
   R.Alias, A.Ibrahim, S.M.Shapee, Z.Ambak, Z.M.Yusoff, M.R.Saad (Telekom Research & Development)/Malaysia
3. Multi-layer Thick Film Circuits with Silver Via Holes Built by All Screen-printing Process
   J.Rufiange (DKN Research)/USA

(16:35)

(16:45)

[16B2-5] Substrate Ⅱ

1. Reliability of Rigid to Flex Interconnection after Reflow
   K.Kawate (Sumitomo 3M)/Japan
2. Low Transmisson Loss and Excellent Heat Resistance Material for Muti-layer PCBs
   Y.Kitai (Panasonic Electric Works)/Japan
3. Development of High Density All Layer IVH PWB with Cavity Structure
   K.Honjo (Panasonic Electronic Devices)/Japan

(18:00)

Room K

[16K-1] RF / RFID Ⅰ

1. Experimental Study of the Isolation Performance of 0.18-um CMOS RF Bond Pad
   M.A.Ismail, N.F.I.Muhammad, A.I.A.Rahim, M.R.Yahya, A.F.A.Mat (Telekom Research & Development)/Malaysia
2. The Thin Type Electromagnetic Wave Absorption Wall Having Optical Ray Passage Property
   Y.Okano (Musashi Institute of Technology)/Japan
3. Development of System that Recognizes Conglomerate RF-ID Tag in UHF Band
   M.Ochiai (Musashi Institute of Technology)/Japan
4. Development of Small Tunable Antenna for Multi-frequency Band
   H.Fukasawa (Musashi Institute of Technology) /Japan

[16K-2] RF / RFID Ⅱ

1. Development of the Meosurement System of Sheet Resistance at Microwave Frequency Range Using DFFC
   T.Tosaka, A.Nishitaka, K.Fukunaga, Y.Yamanaka (NICT)/Japan
2. Evaluation of High Frequency Characteristics of FPC during Bending
   T.Tanaka (Nitto Denko)/Japan
3. Utilizing Scalable Model to Fast Synthesize High Performance RF Integrated Passive Circuits Applited to SiP Module
   C.-C.Wang[1], H.-A.Yang[1], J.Chen[1], T.-C.Lin[1], C.-T.Chiu[1], S.-M.Wu[2], C.-W.Kuo[3], C.-P.Hung[1] ([1]Advanced Semiconductor Engineering, [2]National University of Kaohsiung, [3]National Sun Yat-Sen University)/Taiwan
4. High Performance RF Intergrted Possive Circuits Design on Glass Wafer
   C.-C.Wang[1], H.-A.Yang[1], J.Chen[1], M.-H.Li[2], C.-T.Chiu[1], S.-M.Wu[2], C.-W.Kuo[3], C.-P.Hung[1] ([1]Advanced Semiconductor Engineering, [2]National University of Kaohsiung, [3]National Sun Yat-Sen University)/Taiwan
5. Band Pass Filter Design and Optimization on High-Resistivity Silicon for 5GHz RF Front End Receiver
   Y.Tsuchiya (IBIDEN)/Japan

(12:55)

Lunch time
Poster Session

(13:55)

[16K-3] Reliability

1. Failure Analyses and Lifetime Parameters for Lifetime Monitor of VIA Structures on Printed Circuit Boards
   M.Fujino, T.Suga (The University of Tokyo) /Japan
2. Study on Improving the Drop Impact Reliability of Plastic Core Solder Ball
   R.-D.Sun, N.Okinaga, K.Matsushita, M.Okuda (Sekisui Chemical)/Japan
3. Solder Joint Lifetime Evaluation of WLP and Cause
   T.Matsuzaki (CASIO COMPUTER)/Japan
4. Impact Reliability Studies of Sn-Ag-Cu-Ni BGA Solder Joints on Electroless Ni-P/Au Surface Finish
   F.Kawashiro (NEC Electronics)/Japan
5. Effects of Multiple Reflows on Interfacial Reactions and Shear Strength of SnAgCu Sojder Joints with Cu-Zn Wetting Layer
   Y.M.Kim, S.W.Ma, Y.-H.Kim (Hanyang University) /Korea

(16:00)

(16:10)

[16K-4] Material Ⅱ

1. Eco-fabrication of Noble Metal Nanoparticles by Metal Oxide and Home Electronics Appliances
   Y.Hayashi[1], M.Inoue[2], I.Narita[3], H.Takizawa[1], K.Suganuma[2] ([1]Tohoku Univeristy, [2]Osaka University, [3]Kyushu University)/Japan
2. Preparation and Optical Properties of 30 and 60nm Co_3O_4 Nanowires
   Y.-C.Chen (Feng-Chia University)/Taiwan
3. Molecular Modification of PCB Substrates: Demonstration of HAST Survivability of Fine-Line Patterned Structures
   S.Shi, T.Wei, Z.Liu, C.Rhodine, W.Kuhr (ZettaCore)/USA
4. Development of Thick Resist for Solder Bump
   K.Mori (JSR)/Japan
5. High-speed Power Supply System by Low Characteristic Impedance Transmission Lines Using Metamaterials
   K.Hashimoto[1], Y.Akiyama[1], T.Kawaguchi[2], K.Tahara[2], K.Otsuka[1] ([1]Meisei University, [2]Shin-Etsu Polymer)/Japan

(18:15)

❑Session;
Invited Speeches

Dr. Peter Brofman
(IBM)
Packaging Technology Roadmap - An IBM Perspective

Microelectronic packaging of semiconductor devices is at a crossroad. Conventional scaling of integrated circuitry, which has dominated this industry for over 40 years, has effectively ended. Innovation in materials, design, and packaging will be the engine that will drive the continued performance/cost improvement curve that our customers have come to expect. In this paper, we will examine industry direction in packaging at a high level, and then take a detailed look from an IBM perspective. The latter clearly has a mid- to high-end focus, with an emphasis on the server application application space, although IBM does participate in both games and ASICs markets. From that perspective, we observe a triple convergence of challenges: i) power / thermal management, ii) thermo-mechanical chip-package interaction, and exponential growth in electrical signal bandwidth. These challenges are made more complex by external forces, such as the requirement toward Pb-free materials; use of energy saving system on/off algorithms, and the like.

After exploring the drivers behind the triple convergence, we discuss key examples of technology solutions now being developed to address each of these key challenges, looking at both IBM as well as industry approaches. As noted in last year's keynote address, it is observed that conventional corporate R&D is in general ill-prepared to fund the scope of projects required to address these challenges. Several development business models aimed at addressing this issue will be briefly contrasted. Specifically, IBM and New York State, US have recently announced plans to launch a collaborative Advanced Packaging Development Center, in coordinate with the College of Nanoscale Science & Engineering (CNSE) at Albany State University. The new center will leverage multi-party joint development alliances, similar to the highly successful semiconductor R&D center already established at CNSE. Details of the new Center's mission and status will be discussed.

Mr. Takayuki Watanabe
(Akita Elpida Memory)
The Memory Packaging Strategy with Sophisticated 3D Technology

This paper will discuss memory package technology trend as introducing some new memory package solutions and next generation package.

Currently FBGA (Fine Pitch Ball Grid Array) as commodity memory package is popular in PC/server application area etc. On the other hand, packaging trend for mobile phone, smart phone or digital consumer application requires smaller, thinner and more multi-die/package solution as MCP, PoP and SiP from space or height constraint on application board. But these are still evolved or innovated toward much smaller, much thinner and much multi-die package.

As "Much smaller package technology", this candidate is ideally WLCSP(Wafer level Chip Scale Package). But this CSP is not with big position due to less size compatibility and standardization issue. ALCSP(Advanced Laminated CSP) is introduced here as suitable CSP for semiconductor memory without wafer yield concern on behalf of WLCSP.

As "Much thinner package technology", this requires much thinner die thickness. The thinner package and die are, the more package warpage and memory characteristics instability as refresh time of DRAM are influenced. These might come from mechanical stress due to the difference among thermal expansion characteristics of imbalanced package structure. Here is some package structure approaches to improve and minimize package warpage or memory characteristics influence.

As "Much multi-die package technology", innovative new packaging technology with TSV CoC(Chip on Chip technology with Through Silicon Via) will lead future advanced packaging on behalf of MCP(Multi Chip Package) and SiP(System in Package). Here is new ultra large capacity DRAM consist of multi DRAM cores and interface chip with Copper base TSV interconnection.

Dr. Tetsuroh Muramatsu
(Sharp)
Photovoltaic as An Energy Solution

Ever since the industrial revolution, human civilization has continued to evolve through the invention and spread of technology, be it means of transportation such as automobiles, ships, and planes, or other developments such as communications, broadcasting, and electronics products. In particular, a ubiquitous society centered around developments like the Internet and mobile phones has brought the world closer together. The energy driving all of these developments is solar power and the Earth's minerals. As the world's population increases and civilization's growth slows down, humankind is facing the depletion of fossil fuels and minerals. Today, it has become crucial that we strive to efficiently create electricity from the sun, wind, water, and heat, and distribute this electricity evenly throughout the world. Key to this will be highly efficient solar cells and storage batteries, as well as low-load turbines. In this lecture, we would like to talk about the outlook for solar power generation, what must be done to spread its use, and how this can be done. We will also touch on how electronic packaging technology holds the key to supporting solar power generation.

Oral Session (more than 170 technical papers)

3D/TSV* / Automotive Electronics, Challenges* / Automotive Electronics, Future Requirements* / Embedded Substrate* / High Performance Flip-Chip Packaging* / Fine MEMS* / Assembly Technology for MEMS* / MEMS/TSV Key Technologies* / Printed Electronics* / SiP/PoP Advanced Assembly* / Advanced Packaging / Electrical Solutions / Energy/Environment / Interconnections / LED / Lead Free/Environment / Material / Mechanical Solutions / MFG/Process / Optoelectronics / Reliability / RF/RFID / Substrate / Thermal Management

*Core Session

Poster Session (20 Posters)

P-01 Reliability Evaluations of Flip Chip Packages Using the Digital Image Correlation Method and the FEM Analyses
T.Kanno[1], N.Shishido[1], T.Ikeda[1], N.Miyazaki[1], H.Tanaka[2], T.Hatao[2] ([1]Kyoto University, [2]Sumitomo Bakelite)

P-02 Packaging Stress-induced Shifts of the Electronic and Optical Characteristics of Thin Film Devices Used for Opto-Electronic Hybrid-Integrated Modules
H.Kishi, K.Suzuki, H.Miura (Tohoku University)

P-03 Thermal History Dependence of Mechanical Properties of Electroplated Copper Thin Films Used for Thin Film Interconnection
N.Murata, K.Suzuki, K. Tamakawa, H.Miura (Tohoku University)

P-04 Numerical Analysis of Transport Phenomena in High Aspect Cavity for Bumps Formation
Y.Koyama, Y.Suzuki, N.Okamoto, T.Saito, K.Kondo (Osaka Prefecture University)

P-05 The Effect of the New Levelers for Cu Via-filling
H.Kuri, N.Okamoto, T.Saito, K.Kondo, M.Bunya, M.Takeuchi (Osaka Prefecture University)

P-06 Fabrication of Copper Circuit Patterns on Glass Substrate Using Photochemical Reduction Process
R.Nakamichi, K.Akamatsu, H.Nawafune (Konan University)

P-07 Formation of ULSI Cu Minute Wiring Through Microcontact Printing Using Silicone
K.Nakajima, K.Akamatsu, H.Nawafune (Konan University)

P-08 A Rotating Ring Disk Electrode (RRDE) Study of Cuprous Thiolate Accelerant Produced by Copper Dissolution
S.Hattori, D.P.Barkey, K.Kondo, N.Okamoto, T.Saito (Osaka Prefecture University)

P-09 Improvement of Adhesion Strength between Under Fill Resin and Polyimide Substrate Through Conducting Surface Treatment on Substrate Resin
O.Kato[1], Y.Kimura[1], M.Chino[2], S.Izawa[2] ([1]Kogakuin University, [2]Misuzu Industries)

P-10 Filler Motion Dynamics in Resin for Flip Chip Micro Interconnects by Self-organization Assembly
K.Ohta, K.Fujimoto, M.Matsushima, K.Yasuda (Osaka University)

P-11 Comparison of Erosion Rates of SUS304 and SUS316 Stainless Steel by Molten Sn-3Ag-0.5Cu Solder
K.Sumiyoshi[1], I.Shohji[1], M.Miyazaki[2], ([1]Gunma University, [2]Nagano Oki Electric)

P-12 Effect of Impurities of Au and Pd on Tensile Properties of Eutectic Sn-Pb Solder for Aerospace Application
Y.Saito[1], I.Shohji[1], N.Nemoto[2], T.Nakagawa[3], N.Ebihara[4], F.Iwase[5] ([1]Gunma University, [2]Japan Aerospace Exploration Agency, [3]Nippon Avionics, [4]NEC TOSHIBA Space Systems, [5]HIREC)

P-13 Development of Joining Technology of Al Alloy Plate and Cu Alloy Pipe for Cooling System of Power Module
I.Oshiro[1], I.Shohji[1], H.Nara[2], N.Otomo[2], M.Uenishi[2] ([1]Gunma University, [2]ATAGO MFG)

P-14 Fabrication of Multiplex Electrodes with Stacked Structure for Nerval Interface
M.Kato[1], Y.Ukita[1], Y.Utsumi[1], E.Blasius[2], K.Masubuchi[3] ([1]University of Hyogo, [2]University Karlsruhe, [3]The University of Tokyo)

P-15 Modeling of Self-face-alignment Process Using Contact Potential Difference
R.Sato, T.Tanemura, G.Lopez, M.Serry, K.Sugano, T.Tsuchiya, O.Tabata (Kyoto University)

P-16 An Architecture of Dynamically Reconfigurable Arithmetic Circuit
H.Shimada, Y.Hayakawa, A.Kanasugi (Tokyo Denki University)

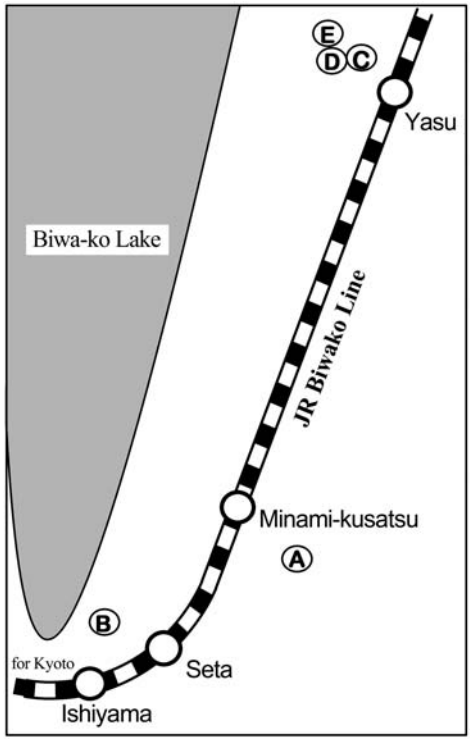
P-17 An Implementation and Verification of Dynamically Reconfigurable Systolic Array
Y.Hayakawa, T.Ishimura, A.Kanasugi (Tokyo Denki University)

P-18 Laser-doppler Velocity Measurements Using An Ultra-compact and Thin Microsensor
S.Nakamura (The University of Tokyo)

P-19 MEMS Type Micro Robot with Artificial Intelligence System
H.Suematsu, K.Kobayashi, R.Ishii, A.Matsuda, Y.Sekine, F.Uchikoba (Nihon University)

P-20 Characterization and Properties of Nanometric-sized SnO_2/CNT Composited Materials for Lithium-Battery Anodes
W.-D.Yang[1], H.-Y.Fang[1], M.-S.Wu[1], H.-M.Tsai[2], C.-S.Hsieh[3] ([1]National Kaohsiung University of Applied Sciences, Kaohsiung, [2]Chung-Shan Institute of Science & Technology, [3]Fooyin University)

❑Plant Tour (Planned on April 17th)



Tour-A RITSUMEIKAN University Biwako-Kusatsu campus
Kusatsu City, Shiga Pref. (Close to Minami-Kusatsu Station on JR BIWAKO line)
MEMS Laboratory & Synchrotron Radiation Equipment Tour

Tour-B TORAY Engineering Co., Ltd.
Ohtsu City, Shiga Pref. (Close to Seta Station on JR BIWAKO line)
Assembly Equipment Manufacturing Plant Tour

Tour-C SONY Mobile Display Corporation
Yasu City, Shiga Pref. (Close to Yasu Station on JR BIWAKO line)
Flat Panel Display Production Plant Tour

Tour-D KYOCERA SLC Technologies Corporation
Yasu City, Shiga Pref. (Close to Yasu Station on JR BIWAKO line)
High Density Circuit Board & Carrier Production Plant Tour

Tour-E OMRON Corporation
ELECTRONIC COMPONENTS COMPANY MICRO DEVICE DIVISION
Yasu City, Shiga Pref. (Close to Yasu Station on JR BIWAKO line)
MEMS&CMOS Production Plant Tour

Please accept below to attend the tour

[1] Attendee Qualification
1. Must not be Competitor
2. Register with ICEP2009 by March13th, 2009 and Apply to the tour

[2] No additional fee is required to attend the tour.
[3] You can attend one tour above. At your application, please input your desired order to attend.
30-50 participant will be accepted for each tour in order of registration receipt.
[4] Registered information will be sent to visiting Company/University.

❑Registration Fees; (Advance by March 31, 2009)

Member (JIEP, IEEE)..... 40 000yen [47 000yen] (Including Reception and Proceedings)
Non Member .....50 000yen [57 000yen] (Including Reception and Proceedings)
Student ..... 5 000yen [5 000yen] (Including Proceedings)
Welcome Reception Only 8 000yen
[ ] At door

❑Committee

General Chair
Hideyuki Nishida (NEP Tech. S&S)
Vice General Chair
Yasumitsu Orii (IBM Japan)
Masato Nakamura (Hitachi)
Advisory
Hironori Asai (Toshiba)
Sei-ichi Denda (Nagano Prefectural Institute of Technology)
Yoshitaka Fukuoka (WEISTI)
Kaoru Hashimoto (Meisei University)
Fumio Miyashiro (Yokohama Jisso Consortium)
Hideyuki Oh-hashi (Mitsubishi Electric)
Kanji Otsuka (Meisei University)
Yuzo Shimada (NEC)
Tadatomo Suga (The University of Tokyo)
Haruo Tabata
Shinichi Wakabayashi (Shinko Electric Industries)
Itsuo Watanabe (Hitachi Chemical)
Kishio Yokouchi (Fujitsu Interconnect Technologies)
TPC Chair
Yasumitsu Orii (IBM Japan)
TPC Vice Chair
Yasuhiro Ando (Fujikura)
Nobuaki Hashimoto (Seiko Epson)
Shoji Uegaki (ASE Marketing & Service Japan)
TPC Member
Masahiro Aoyagi (National Institute of Advanced Industrial Science and Technology)
Tomoyuki Abe (Fujitsu Laboratories)
Masazumi Amagai (Texas Instruments Japan)
Shigeru Hiura (Toshiba)
Hiroshi Hozoji (Hitachi)
Kinya Ichikawa (Intel)
Toru Ikeda (Kyoto University)
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