Advance Program

2004 ICEP

"Nanotechnology Coming up"

International Conference on Electronics Packaging
(Formerly IEMT/IMC Symposium)

April 14-16, 2004
Dai-ichi Hotel Tokyo Seafort
Tennoz Isle, Tokyo, Japan

Sponsored by

IMAPS Japan (International Microelectronics and Packaging Society Japan) / **JIEP** (Japan Institute of Electronics Packaging)
IEEE CPMT (Components, Packaging, and Manufacturing Technology) **Society Japan**

Welcome to 2004 ICEP

On behalf of the Conference Organizing Committee, I cordially welcome you to 2004 International Conference on Electronics Packaging (ICEP) which is jointly sponsored by IEEE CPMT (Components, Packaging, and Manufacturing Technology) Society Japan and IMAPS Japan (International Microelectronics and Packaging Society Japan) / JIEP (Japan Institute of Electronics Packaging). It is a valuable opportunity to enrich your research and development activities or professional skills with the latest information. Looking back to last year, 2003 ICEP was significantly influenced by SARS and the Iraq War. However, the conference was successful thanks to the vital assistance extended by many participants to the organizing committee and technical program committee. For example, some chaired sessions or acted as speakers in lieu of participants who unexpectedly cancelled. I greatly appreciate the assistance and efforts that were so forthcoming from numerous participants, especially those from overseas. I earnestly hope that 2004 ICEP will run smoothly without any adverse influences.

There is growing recognition that nanotechnology is destined to have a tremendous impact in scientific and technological fields. At the conference, one of our invited speakers will address the subject of nanotechnology. Several presentations in other sessions also concern nanotechnology. The catchphrase of 2004 ICEP is "Nanotechnology Coming up". In addition, we will illuminate new approaches to integration of the currently diverse microelectronics packaging technologies, through a series of thirteen sessions: Advanced Packaging, Reliability and Test, Substrates/Interposer, Opto-electronics, Interconnection, Materials, Thermal Management, MEMS Packaging, Lead free, Flip-chip, High Speed Board Design, System in Package and Business/Trend. The Business/Trends session will also provide you with useful information on the industry. 2004 ICEP will be a golden opportunity for all of us to look into the future of packaging technology and the associated business developments.

In addition to the conference, the Microelectronics Show held at Tokyo Ryutsu Center will keep you abreast of the latest developments in materials, equipment and commercialized technologies in your field of interest. I urge you to tour the exhibition and ask any questions you may have concerning products or technologies.

I would like to express my gratitude to the members of the Organizing Committee who have all worked so hard to ensure this conference is a resounding success. It will be a valuable opportunity you won't want to miss. See you at Tennoz Isle in Tokyo!

Yoshitaka Fukuoka
General Chairperson

GENERAL INFORMATION

International Conference on Electronics Packaging (ICEP), the largest international conference in Japan focusing on the field of electronics packaging, has been held annually for two decades. The conference consists of twelve technological topics and one business & trends session.

At ICEP, participants can easily acquire the latest information on electronics packaging. Major trends concerning IT are highlighted. This is a golden opportunity to gather a wealth of valuable information and engage in fruitful discussion with fellow professionals on the latest developments in electronic packaging.

CONFERENCE

Eighty-six papers will be presented in 12 technical and other sessions; Advanced Packaging, Reliability and Test, Substrates/ Interposer, Optoelectronics, Interconnection, Materials, Thermal Management, MEMS Packaging, Lead free, Flip-chip, High Speed Board Design, System in Package, and Business/ Trends. Guest speakers will also focus on advanced packaging technologies in the afternoon of April 14.

Room-A, Room-B
The Harbor Circus, 3F.
Dai-ichi Hotel Tokyo Seafort

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Mamoru Kurashina (Fujitsu Laboratories)
Masato Nakamura (Hitachi)

* Chairperson ** Vice Chair

April 14 (Wed.)

10:00

WA1: Advanced Packaging

Chairperson: R. Aschenbrenner (IZM)
H. Nishida (International Display Technology)

1. **Ambient Intelligence and Embedded Electronics** (Session Invite)
   P. Collander, *Poltronic* / Finland
2. **Unique Semiconductor Packages Developed in Japan** (Session Invite)
   S. Denda, Y. Tezuka, Y. Nishioka, K. Iijima, *Nagano Prefectural Institute of Technology* / Japan
3. Integrated Modeling and Testing of Fine-pitch CSP under Board Level Drop Test, and Thermal Cycling Test
   T.Y. Tee, J. Luan, H.S. Ng, D. Yap, *STMicroelectronics* / Singapore, K. Loh, *Zymet* / USA, E. Pek, C.T. Lim, *National University of Singapore*, Z. Zhong, *Nanyang Technological University* / Singapore
4. Reliability of an Ultra-high-density 3-dimensional-stacked Package "FFCSP"
   Y. Sogawa, T. Yamazaki, I. Hazeyama, S. Kitajo, *NEC*, R. Yoshino, K. Kata, *NEC Electronics* / Japan
5. A Control Circuit for Reconstruction of Wafer Scale Integrated Circuit
   A. Kanasugi, *Tokyo Denki University* / Japan
6. Study on a Fast Prototyping of Chip-On-Film(COF) by Using of AuSu Eutectic Bonding
   T.C. Chau, *Solomon Systech*, Y.C. Chan, *City University of Hong Kong*, W.C. Lai, Y.F. Ho, K.W. Leung, *Solomon Systech* / Hong Kong
7. Comprehensive Process Warpage Analysis of Matrix Stacked Die BGA
   X. Zhang, T.Y. Tee, *STMicroelectronics* / Singapore

WB1: Materials I

Chairperson: M. Otsuka (Shibaura Institute of Technology)
Y. Hatanaka (Mitsubishi Electric)

1. **Fabrication of Metal Green Sheets and their Application** (Session Invite)
   F. Uchikoba, *Nihon University* / Japan
2. Ag-Sn Alloys as Conductive Fillers in ICAs
   Y. Shirai, *Namics*, K. Suganuma, *Osaka University*, N. Mizumura, *Namics* / Japan
3. High Strength Alumina Ceramic Material for Surface Mount Packages
   M. Izumi, T. Hasegawa, S. Yamada, M. Kokubu, *Kyocera* / Japan
4. UBM Formation Using Improved Double Zincating Process
   S. Kawashima, *Meltex* / Japan
5. Is the Residual Silicone Fatal to Semiconductor Packaging?
   K. Nagamoto, *Lintec* / Japan
6. Black Solder Resist Issue in Manufacturing Printed Circuit Board for Flash Memory Card
   K.-S. Lee, K.-Y. Kim, K.-H. Lim, D.-G. Yang, B.-H. Rhee, *Samsung Electro-Mechanics* / Korea
7. UV Curing and Electrical Characterization of Chip on Flex for Smart Card Applications
   B. Y. Ma, *City University of Hong Kong*, C. F. Luk, *Optimal Technology*, Y. C. Chan, *City University of Hong Kong* / Hong Kong

12:55

LUNCH TIME

14:00

WELCOME SPEECH

14:15

AWARDING CEREMONY

14:30

Invited Speech

Chairperson: Y. Fukuoka (Weisti)
I. Watanabe (Hitachi Chemical)

1. **It is a Small World- the Nano Science and Technology in Electronic Packaging**
   C. P. Wong
   Georgia Institute of Technology / USA

2. **New and Emerging Technologies for System Integration**
   R. Aschenbrenner, J. Wolf, H. Reichi
   IZM / Germany

3. **Electronics Packaging Considerations for Space Applications**
   P. J. Zulueta
   President of IMAPS, California Institute of Technology / USA

17:00

18:00

WELCOME RECEPTION

The Harbor Circus
Dai-ichi Hotel Tokyo Seafort, 3F.

20:00

WELCOME SPEECH

2:00 p.m., Wednesday, April 14
Room-A+Room-B
The Harbor Circus, 3F.
Dai-ichi Hotel Tokyo Seafort

The welcome speech is scheduled for the beginning of the afternoon session on April 14. Dr. Fukuoka, the general chairperson for 2004 ICEP, will welcome the participants and comment on the significance of the conference.

AWARDING CEREMONY

2:15 p.m., Wednesday, April 14
Room-A+Room-B
The Harbor Circus, 3F.
Dai-ichi Hotel Tokyo Seafort

2003 ICEP technical program committee carefully examined and screened all the papers presented at the last conference. The committee selected several excellent papers. The authors of those papers will be congratulated at this ceremony by the President of JIEP.

The "Young Award" has been established in order to encourage the work of young researchers. The award is intended for those aged under thirty-five. Those distinguished younger researchers will be also congratulated by the General Chairperson of IEEE CPMT Japan Chapter.

WELCOME RECEPTION

6:00-8:00 p.m., Wednesday, April 14
The Harbor Circus, 3F.
Dai-ichi Hotel Tokyo Seafort

A welcome reception is scheduled after the opening day session at the Harbor Circus, which is at Dai-ichi Hotel Tokyo Seafort. Almost all of the conference participants attend the reception. This is an excellent chance to cultivate relationships with counterparts from Japan and around the world and to exchange useful information. A ticket is included with your conference registration. Additional tickets may be ordered using the registration form.

April 15 (Thu.)

9:00

TA1: Substrate / Interposer I

Chairperson: E. Zakel (Pac Teck)
S. Uegaki (Kyocera)

1. Surface Treatment of a Photo Sensitive Insulation Layer for a Robust Build up Printed Circuit Board
   T. Yabuuchi, *Kyocera SLC Technologies* / Japan
2. High Frequency Properties of the MLTS
   K. Nakase, J. Sakai, T. Shimoto, H. Inoue, *NEC* / Japan
3. Development of Buried Bump Interconnection Technology with Embedded Passive Devices
   S. Shibasaki, T. Serizawa, T. Kihara, *Dai Nippon Printing*, K. Sasaoka, N. Morioka, *D. T. Circuit Technology*, Y. Yamaguchi, K. Shinozaki, *Dai Nippon Printing*, Y. Fukuoka, *Worldwide Electronic Integrated Substrate Technology* / Japan
4. Green Sheet for Photolithography
   F. Uchikoba, Nihon University / Japan
5. Fabrication Process and Characterization of the OSP(Organic Solderability Preservatives) Finished CSP Substrate for Mobile Applications
   H.S. Lee, C.H. Kim, Y.H. Shin, B.H. Rhee, *Samsung Electro-Mechanics* / Korea
6. Development of Dynamic Test Board in Numerical and Experimental Investigation
   H.T. Yang, *Intel Technology* / Malaysia

11:30

TB1: Materials II

Chairperson: B. Vandecasteele (IMEC)
I. Kaneko (Musashi Institute of Technology)

1. **Self-Organized ACP Interconnection Using Wetting Property of Fusible Fillers** (Session Invite)
   K. Yasuda, *Osaka University* / Japan
2. Development of Ecological Membrane Switch
   K. Ishida, *Fujikura* / Japan
3. Implementation of Skip-Cure Die Attach Paste on Wire Bonding Process
   Y. Uematsu, *Henkel Loctite* / USA
4. Organic Spacers in Die Attach Pastes for Bondline Contorol in Semiconductor Packages
   C. Perabo, C. Cottonaro, *Henkel Loctite*, P. Stoessel, *ESEC USA* / USA
5. High Thermal Conductivity Materials: Synthesis of AlN and Its Applications in Substrates and EMC
   C.-N. Lin, C.-Y. Hsieh, C.-W. Chang, S.-L. Chung, *National Cheng Kung University* / Taiwan
6. The New Integrated Microelectronic Intelligent Lighting System Based on the Hybrids Controllers
   J. Gondek, *Private Institute of Electronic Engineering*, S. Kordowiak, *Cracow University of Technology*, J. Kocol., *Technical School of Telecommunication* / Poland

LUNCH TIME

12:30

TA2: Substrate / Interposer II

Chairperson: P. Jalonen (Satakunta Polytechnic)
F. Uchikoba (Nihon University)

1. New Process of Manufacturing Printed Circuit Boards Using Electrophotography Technology
   N. Yamaguchi, *Toshiba* / Japan
2. Combining Power and Microelectronic Circuits on One Single Substrate
   J. Schulz-Harder, *Curamik Electronics* / Germany
3. Improvement of Interfacial Adhesion of Polyimide/Epoxy Using Plasma Treatment for High Performance Flexible Printed Circuit
   B.Y. Myung, Y.P. Park, D.J. Yang, B.H. Rhee, *Samsung Electro-Mechanics* / Korea
4. Electrical Properties of TaN-Cu Nanocomposite Thin Films
   J.H. Hsieh, C.M. Wang, C. Li, Y.Q. Fu, *Nanyang Technological University* / Singapor
5. The Advantage of Fine Finger Pitch PBGA Substrate
   D. Chang, Y.P. Wang, C.S. Hsiao, *Siliconware Precision Industries* / Taiwan
6. New Multi-layer Manufacturing Techniques for High Density, High Performance Printed Circuit Boards
   T. Kim, *Samsung Electro-Mechanics* / Korea

15:00

TB2: Reliability & Test

Chairperson: C. Zardini (Universite Bordeaux I)
H. Hozoji (Hitachi)

1. **Study and Applications of the Low Temperature Lead-free Soldering** (Session Invite)
   J. Ma, *Tsinghua University* / China
2. Probing CSP's: Not Front End, Not Back End
   T.Q. Collier, *CV* / USA
3. Understanding Probing on Package Performance Front-Back Issues
   T.Q. Collier, *CV* / USA
4. Effect of Moisture Absorption on Reliability of ACF Interconnects between FPC and Glass Substrates
   M. Inou, T. Miyamoto, K. Suganuma, *Osaka University* / Japan
5. AC Electric Field for Detecting Pin Opens by Supply Current of CMOS ICs
   M. Takagi, *Takuma National College of Technology*, M. Hashizume, M. Ichimiya, *The University of Tokushima* , I. Tsukimoto, *Takuma National College of Technology*, H. Yotsuyanagi, T. Tamesada, *The University of Tokushima* / Japan
6. Evaluation of Residual Stress in Resin Molding IC Chips Using FEM
   M. Koganemaru, *Fukuoka Industrial Technology Center* / Japan

COFFEE BREAK

15:15

TA3: Optoelectronics

Chairperson: S. Priyadarshi (Luminent)
S. Yoshida (Tokyo Institute, Polytechnic University)

1. Opto-electronic Chip-on-film Packaging Technology Using Fluorinated Polyimide Optical Waveguide Films
   M. Usui, S. Ishibashi, H. Hirata, S. Ishizawa, N. Koshoubu, T. Hayashi, S. Ohki, *NTT* / Japan
2. Novel Polyimide Waveguide Fabricated by the Femtosecond Laser Pulses
   F. Sezaki, K. Namura, *Kaneka*, K. Kamada, K. Kintaka, J. Nishii, *National Institute of Advanced Industrial Science and Technology* / Japan
3. Improvement of Interfacial Adhesion of Al/Cr Films Deposited on Indium Tin Oxide Coated Glasses by Interfacial Oxidation
   T.-M. Wu, J.-Z. Tong, *National Chung Hsing University*, J.-H.J. Hsieh, *Nanyang Technological University*, Y. S. Yang, *Metal Industries Research and Development Center* / Taiwan

16:30

TA4: Business / Trends

Chairperson: C. Bauer (TechLead)
K. Hashimoto (Fujitsu Laboratories)

1. Packaging Technology & Market Trends in Taiwan
   S. L. Fu, *I Shou University* / Taiwan
2. Microelectronics Industry Management Strategies; an Updated EU Perspective
   A. Gandelli, *Politecnico di Milano* / Italy
3. Strengthening the Electronics Manufacturing Supply Chain
   R. Pfahl, J. McElroy, *NEMI* / USA

17:45

TB3: Flip Chip

Chairperson: E. J. Vardaman (TechSearch)
T. Satoh (Sharp)

1. **Low Cost Electroless Bumping for Ultra Fine Pitch Application in 8" and 12" Wafers** (Session Invite)
   E. Zakel, *Pac Tech* / Germany
2. **Capillary Chip Connection (C3); Low Cost Flip Chip Solution?** (Session Invite)
   C.E. Bauer, *TechLead* / USA, A. Taran, *Microelectronic Assembly Innovations* / Russia
3. Processing and Electrical Property Studies of Conductive Adhesives Filled with Metallic Particles and the Effect of the Additions of Nano-sized Metallic Particles
   L.-C. Chen, H.-W. Chiang, C.-L. Chung, S.-L. Fu, *I-Shou University* / Taiwan
4. Plastic Flip-chip MMIC Package for Millimeter-wave Application
   S. Masuda, *Fujitsu Laboratories*, H. Kira, M. Kitajima, *Fujitsu* / Japan
5. Improvements of a Board Level Reliability of the W-CSP with Lead Free Solder Using Stress Analysis
   S. Tanaka, *Seiko EPSON* / Japan
6. Failure Mode Analysis by Non-destructive Evaluation and EBSP Technique
   K. Ueno, *Kobelco Research Institute* / Japan

INTERNATIONAL RECEPTION

Evening, Thursday, April 15
Dai-ichi Hotel Tokyo Seafort
(Overseas attendance only)

All participants from overseas are welcome to attend the International Reception. This is an informal event where you can relax and develop friendships with fellow professionals from around the world.

Registration Fees

Member & Speaker	40 000yen (35 000yen)*
Student	5 000yen**
Non Member	50 000yen (45 000yen)*
Accompanying Spouse	5 000yen
Welcome Reception Only	8 000yen
Extra Proceedings	10 000yen

*Including Reception and Proceedings
**Including Proceedings
( ) Advance by March 20, 2004

April 16 (Fri.)

FA1: Interconnection

Chairperson: K. Hashimoto (Fujitsu Laboratories)
M. Tsukamoto (The University of Tokyo)

1. LCP / Cu Lamination by the Surface Activated Bonding (SAB)
   K. Nanbu, *Toyo Kohan* / Japan
2. Novel Material System Solution for Fine Pitch Non-metallurgical Flip Chip Interconnections
   N. Tanaka, *Hitachi*, A. Nagai, M. Yasuda, *Hitachi Chemical* / Japan
3. Interconnection Sheet for Ultra High Pin Counts Applications
   T. Ochiai, K. Miwa, K. Taguchi, *NGK Insulators* / Japan
4. Resin Encapsulated Flex Interconnection
   K. Kawate, *Sumitomo 3M* / Japan
5. Low Temperature Flip Chip Attachment for Flexible Display Applications
   B. Vandecasteele, *IMEC*, J. Maattanen, *Elcoteq Network* / Finland,
   T. Podprocky, J. Vanfleteren, *IMEC* / Belgium
6. Development of Void Decrease Process in BGA/CSP Mounting
   M. Takesue, *Fujitsu* / Japan

11:30

FB1: Highspeed Board Design

Chairperson: P. Collander (Poltronic)
S. Hiura (Toshiba)

1. Design for Enhanced Board Level Solder Joint Reliability of Very High Pin Count FCBGA Package
   H.S. Ng, M. Lim, T.Y. Tee, *STMicroelectronics* / Singapore
2. Electrical Modeling of FC-BGA for High Speed Package Applications
   M.-K. Chen, C.-C. Tai, *National Cheng Kung University*,
   Y.-J. Huang, S.-L. Fu, *I-Shou University* / Taiwan
3. A Simulation Methodology and Design Practice for High Speed Parallel Bus Considering SSN
   N. Takahashi, S. Suminaga, *IBM Japan* / Japan
4. Compact Vertical Transitions for High-speed Printed Circuit Boards
   T. Kushta, K. Narita, T. Saeki, H. Tohya, *NEC* / Japan
5. Improvement of LAN Cable for 1Gbps Ethernet with High Frequency of 300MHz
   O. Koyasu, K. Ohashi, *Fujikura*, Y. Akiyama, K. Otsuka, *Meisei University* / Japan
6. Measurements of the Transmission Characteristics and the Electric Field Radiation of Various Parallel Pair Lines
   T. Kasuga, E. Ohta, K. Takahashi, H. Inoue, *Akita University* / Japan

LUNCH TIME

12:30

FA2: MEMS Packaging

Chairperson: A. Okuno (Sanyu Rec)
N. Hashimoto (Seiko Epson)

1. Packaging and Assembly of MEMS Devices: A Major Impediment to the Industry
   A. Morita, *Prismark Partners* / USA
2. Aligned Room-temperature Wafer Bonding by Ar Beam Surface Activation for Wafer-scale MEMS Packaging
   H. Takagi, *National Institute of Advanced Industrial Science and Technology* / Japan
3. Novel Packaging Technology for MEMS Devices
   M. Chino, T. Shimada, H. Tazawa, *Misuzu Industries*,
   M. Urano, H. Ishii, T. Shimamura, K. Machida, *NTT* / Japan
4. A Novel MEMS Optical Fiber Pressure Sensor Packaging Design
   G. Wang, Y. Fu, M E Welland, H.P. Hodson, *University of Cambridge*, / UK,
   J. Ma, *Tsinghua University* / China
5. Dicing Technology for the Next Generation – The Stealth Dicing Technology
   F. Fukuyo, *Hamamatsu Photonics* / Japan

14:35

FB2: Thermal Management

Chairperson: H.-S. Ng (STMicroelectronics)
S. Kitajo (NEC)

1. **Evaluation by Simulation of the Aging State of a Thyristor System Used in a Power Plant** (Session Invite)
   A. Guedon-Gracia, E. Woirgard, **C. Zardini,** *Universite Bordeaux I*,
   G. Simon, *EDF R&D site les Renardieres* / France
2. Wick Structure Effect on the Performance of Vapor Chambers
   C.-W. Lin, J.-C. Shyu, L.-K. Yeh, S.-W. Chen, C.-T. Chou, M.-J. Tsai,
   Industry Technology Research Institute / Taiwan
3. Thermal Fatigue Life Prediction of Sn-3.0Ag-0.5Cu Solder Joint by Modified Coffin-Manson Equation
   M. Yamabe, *Toshiba* / Japan
4. Thermal Performance of Stacked CSPs
   G. Gray, S. Krishnan, I. Osorio, *Tessera* / USA
5. Comparative Study of Thermally Conductive Fillers in Underfills
   W.-S. Lee, J. Yu, *Korea Advanced Institute of Science and Technology*,
   T.Y. Lee, *Hanbat University* / Korea

COFFEE BREAK

14:50

FA3: System in Package

Chairperson: S.-L. Fu (I-Shou University)
Y. Kodama (Kyocera SLC Technologies)

1. First Single Module Demonstration of SOP with Digital, Optical and RF for Last Mile Broadband Applications
   V. Sundaram, R.R. Tummala, *Georgia Institute of Technology* / USA
2. Development of a New Interposer Including Embedded Film Passive Components
   K. Nakamura, T. Mori, K. Nakayama, M. Yamaguchi, M. Akazawa, S. Kuramochi,
   A. Takano, *Dai Nippon Printing*, Y. Fukuoka, *Weisti* / Japan
3. FCBGA Type High Speed SIP using Ultra Fine Pitch Interposer
   H. Matsuki, T. Okamoto, M. Ikumo, S. Tiba, N. Saito, A. Miyota, E. Watanabe,
   Fujitsu / Japan
4. Polymeric Carbon Embedded Resistors in Multilayer Printed Wiring Boards
   K. Perala, T. Rapala-Virtanen, *Aspocomp Group*,
   T. Uusluoto, A. Tuominen, *Tampere University of Technology* / Finland
5. An Alternative Method for Organic Substrate for Use in High Density Miniaturized Electronic Assembly
   P. Jalonen, *Satakunta Polytechnic* / Finland
6. New Approaches to 3-D Interconnection Systems in Package Applications
   C. Val, *3D Plus* / France

17:20

FB3: Lead Free

Chairperson: G. Gray (Tessera)
K. Tsunoi (Fujitsu)

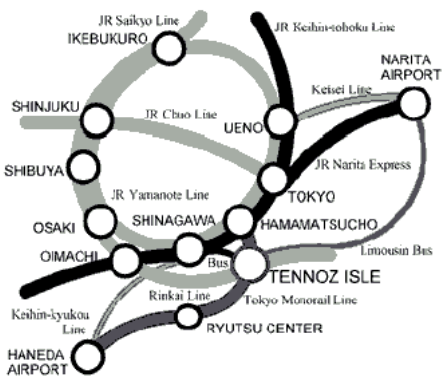
1. Development of New Fluxless Reflow Soldering Process by Hydrogen Radical
   T. Nakamori, *Kumamoto University* / Japan
2. Effect of Aging on the Interfacial Reaction of BGA Sn-Ag-Cu and Sn-Ag Solders with Ni(P)/Au Surface Finish on Pad
   A. Sharif, Y.C. Chan, *City University of Hong Kong* / Hong Kong
3. Comparative Study of Lead Free Solder with Electrolytic Ni and Electroless NiP Layer during Long Time Reflow on BGA Packages
   M.N. Islam, Y.C. Chan, *City University of Hong Kong* / Hong Kong
4. Analysis on the Surface Oxide Film and the Reliability of Bumps Used for Flip Chip Bonding
   Y. Liu, J. Ma, G. Chen, Q. Li, *Tsinghua University* / China
5. Comparison of Wire Bondability on Rigid and Flexible Substrates
   Y.H.Chan, J.-K. Kim, *Hong Kong University of Science & Technology*,
   D. Liu, P.C.K. Liu, Y.M. Cheung, M.W. Ng, *ASM Assembly Automation* / Hong Kong

(16:55)

MICROELECTRONICS SHOW

State-of-the-art technologies, materials, devices, and equipment for microelectronics will be displayed at the 18th Microelectronics Show, which will be held at Tokyo Ryutsu Center(TRC) during the same period. Numerous leading companies will be exhibiting cutting-edge technologies and products.

10:00a.m. - 5:00p.m. Wednesday, April 14
10:00a.m. - 5:00p.m. Thursday, April 15
10:00a.m. - 4:00p.m. Friday, April 16
(Admission Free)
Tokyo Ryutsu Center
(The 2nd monorail station from the Conference site)



For more information on 2004 ICEP
contact :
Secretariat of 2004 ICEP
IMAPS Japan / JIEP
3-12-2 Nishiogikita, Suginami-ku
Tokyo 167-0042, Japan
Phone:+81-3-5310-2010, Facsimile:+81-3-5310-2011
E-mail : imaps-j@jiep.or.jp

2004 ICEP事務局
社団法人エレクトロニクス実装学会
〒167-0042 東京都杉並区西荻北3-12-2
電話:03-5310-2010, FAX:03-5310-2011