Official Program

ICEP 2021 International Conference on Electronics Packaging

2021 International Conference on Electronics Packaging (ICEP)

May 12-14, 2021

All-Online Event

Sponsored by JIEP. Technical Co-Sponsored by IEEE EPS Japan Chapter and iMAPS

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The Japan Institute of Electronics Packaging (JIEP)

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IEEE EPS Japan Chapter
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Welcome to ICEP 2021

On behalf of the organizing committee, we take great pleasure in welcoming you to the 20th International Conference on Electronics Packaging (ICEP) May 2021, held for the first time as an all-online event. The conference is sponsored by the Japan Institute of Electronics Packaging (JIEP) and technically co-sponsored by the IEEE Electronics Packaging Society (EPS) Japan Chapter and International Microelectronics Assembly & Packaging Society (IMAPS).

ICEP is a major conference in the field of electronics packaging and regularly attracts around 400 participants. It has a long history dating back to the International Microelectronics Conference (IMC) in 1980. The IMC sponsored by the International Society for Hybrid Microelectronics (ISHM) Japan was first held in 1980 before the establishment of JIEP (1998). It was held every second year until 1997. In 1997, it merged with the IEEE International Electronic Manufacturing Technology Symposium (IEMT) to become the annual IEMT/IMC. In 2001, it was renamed to ICEP and has been held annually ever since. Every three years since 2012, it has been organized with the IMAPS All Asia Conference (IAAC). Unfortunately, last year's conference was canceled for the first time ever to prevent the spread of COVID-19. Since the pandemic spread shows no signs of abating soon, the organizing committee has decided to transform the in-person ICEP 2021 that was scheduled to be held in the Miraikan (The National Museum of Emerging Science and Innovation) in Tokyo into a virtual event. We believe that the online conference can be particularly beneficial during this public health crisis.

The conference will provide excellent opportunities for researchers and engineers from academic and industrial communities worldwide to address new challenges and discuss future research directions in the field of electronics packaging. The scope of the conference covers a wide range of topics like advanced packaging, design, modeling and reliability, emerging technologies, high-speed wireless components, thermal management, interconnections, materials and processes, optoelectronics, and power electronics. The online ICEP 2021 has two segments: live and on-demand online sessions. This high-skill technical program will include five acclaimed keynote lectures by internationally renowned speakers, session invited presentations on cutting-edge topics, and approximately 100 contributed oral/poster presentations. This year also marks a special occasion, as the ICEP celebrates its 20th anniversary. To commemorate this, this year’s conference will feature a special lecture focusing on “Challenges and Future Directions in the Semiconductor Industry.” An electronic copy of the 20th anniversary DVD containing all the papers of previous ICEPs (2001–2019), will be distributed to all the participants of ICEP 2021.

Finally, we would like to thank our sponsors, committee members, session chairs, authors, and presenters for their contributions, as well as the secretariat members for their assistance and support over the past years in planning this conference.

We sincerely hope that you will enjoy all the inspirational talks and discussions at the virtual ICEP 2021.

E. Higurashi

Eiji Higurashi
General Chair, ICEP2021

ICEP 2021 Keynote Lectures

Comprehensive SiP Enabling New System Integration

Chih-Pin Hung
Vice President of Corporate R&D,
ASE Group

Advanced System in Package (SiP) is offering the system developer comprehensive solutions to differentiate their products to meet various components integration needs. This talk will discuss innovations in SiP technologies – embedded, Flip-Chip, and Fan-Out, describing how the needs are achieved with higher density, smaller form factor and shortened design flow, so very essential for new decade AIoT, 5G, automotive and data center applications.

■ Biography

Dr. CP Hung currently holds the position of Vice President, Corporate R&D, at ASE Group. Based in Kaohsiung, Taiwan, he leads teams responsible for next-generation product development featuring integrated technologies, as well as a broad range of advanced chip, package, and system integration solutions.
During his tenure, Dr. Hung has performed a variety of management roles at ASE, including VP of Corporate Design, VP of Central Engineering & Business Development and VP of Logistic Services Integration. He holds 88 patents encompassing IC packaging structure, process, substrate and characterization technology. He has also published over 62 conference and journal papers.
Dr. Hung has being the SEMICON Taiwan PKG & TEST Committee Chair since 2013, IEEE EPS Board of Governor since 2019.

Future View: technology merger strengthens evolution of semiconductor chips in the hyper-scaling AI/ML era

Kazuya Okamoto
Yamaguchi University
Osaka University

The industry has historically evolved along an S-shaped growth curve and could be explained by Rogers' normal distribution using a diffusion of innovation theory. However, this distribution is changing in the current contestable market created by Big Tech like GAFAM (Google, Amazon, Facebook, Apple and Microsoft). The semiconductor industry, which is a pivotal component of this market, is developing into a new model quite different from the conventional one, especially under the Covid-19 epidemic.

In this keynote lecture, we discuss what a semiconductor should be in the future, based on inductive strategic thinking using IP (Intellectual Property) information and other resources. Specifically, we will review crucial items in the AI/ML (Artificial Intelligence/Machine Learning) era including: 1) Increased costs to shrink transistors and modify their structures, 2) Transition to various 3D strategies to reduce RC delay and power consumption in the interconnects, and to create added value, 3) Importance of integrated metrology using AI/ML, and 4) Need for an optimal solution in the Heterogeneous Integration that combines the design, fabrication process, and high-density packaging with a chiplet and/or panel level concept.

Today, semiconductor technology drivers are changing from conventional Memory and Logic devices to specialized AI chips, and the technology merger of various kinds of design and fabrication fields supports the evolution of these chips.

■ Biography

Kazuya Okamoto received his Ph.D. degree in electronic engineering from The University of Tokyo, and the Diploma (Executive Education) from the Harvard Business School.
After joining Nikon Corporation, Dr. Okamoto was involved in a multitude of technologies ranging from design to fabrication of CMOS devices for company products. Later, he was engaged in R&D of optical integrated circuits (OIC) and developed a highly efficient coupling method between GaAs/AlGaAs DFB lasers and optical waveguides. He also commercialized a nanometer displacement OIC sensor using mode interference theory. During his tenure as Vice President of Nikon Research and a General Manager of Nikon, Dr. Okamoto and his team developed an innovative e-beam lithography optics with IBM, as well as a precision wafer bonding system equipped with advanced alignment technology, and a macro inspection system using IR light.
In 2005 he became a Visiting Professor with Osaka University, and a technology advisor of the Cabinet Office in Japan. Since 2016, he has been a Professor of Yamaguchi University and a Guest Professor of Osaka University. In 2018, he was in charge of the development of advanced integrated metrology technology utilizing AI/ML as a Chair of the R&D Committee of the Japan Society for the Promotion of Science (JSPS). His current research interests include a new business creation and system design methodology for the future of the semiconductor industry and others.

ICEP 2021 Keynote Lectures

Direct Bonding: A New Paradigm Shift in Semiconductor Assembly

Belgacem Haba
Xperi

Cancelled

Superconducting Circuits for Quantum Technologies

Yasunobu Nakamura
The University of Tokyo
RIKEN Center for Emergent Matter Science

Superconducting circuits are widely investigated for various applications in quantum information technologies these days. Thanks to the drastic improvement of the coherence properties of superconducting qubits in the last two decades, as well as to their large dipole moment and strong nonlinearity that allow fast control and readout, they are considered to be one of the most promising platforms for implementing quantum information processors flexibly designed on-chip. In addition, based on circuit quantum electrodynamics, qubits are coupled to resonators and waveguides to exploit the properties of those bosonic modes, either localized or propagating. In this talk, I will give an overview of the field and introduce our activities.

■ Biography

Yasunobu Nakamura studied physical properties of high-temperature superconductors and received BSc in Department of Applied Physics, The University of Tokyo in 1990 and MSc in Superconductivity Research Course, The University of Tokyo in 1992. He joined Fundamental Research Laboratories of NEC Corporation in 1992 and started working on mesoscopic electronic devices. In 1999 he demonstrated the first coherent control of a superconducting qubit. During 2001-2002, he spent a year in Department of Applied Physics, Delft University of Technology as a Visiting Researcher. He received D. Eng. from Department of Applied Physics, The University of Tokyo in 2011. He moved to the current position in Research Center for Advanced Science and Technology (RCAST), The University of Tokyo, in 2012. He is also affiliated to RIKEN Center for Emergent Matter Science as a Team Leader of Superconducting Quantum Electronics Team since 2014. He has been the Director of ERATO Macroscopic Quantum Machines Project of Japan Science and Technology Agency (JST) since 2016 and the Project Leader of Q-LEAP Flagship Project on Superconducting Quantum Computers since 2018. His current research interests are quantum information processing using superconducting circuits, microwave quantum optics, and hybrid quantum systems. He has received Sir Martin Wood Prize and Nishina Memorial Prize in 1999, Agilent Technologies Europhysics Prize in 2004, Simon Memorial Prize in 2008, Leo Esaki Prize in 2014, and Japan Society of Applied Physics Outstanding Achievement Award in 2019.

Progress of Wafer Level Packaging Technology for RF Devices at 5G Era

Daquan Yu
Xiamen University

As Moore's Law is reaching the limitation, the developing of advanced packaging technology towards to advanced system integration will play key role for semiconductor industry. The development of wafer level packaging technology provides strong support for 5G device integration to meet miniaturization, high performance and low cost. Wafer level Fan-in can be used for SAW/BAW filters and IPD, RF modules. Wafer Level Fan-out can be used for RF modules and mmWave chips. Recently, glass wafer level packaging using through glass via (TGV) technology and embedded glass fan-out (GFO) technology become more and more mature, which can be used for 3D integration for IPD, mmWave, RF module. The advantages of glass wafer packaging include small form factor, low cost, simple process, and excellent electrical performance. This talk will discuss the technologies and challenges of the advanced wafer level manufacturing processes for various 5G applications.

■ Biography

Dr. Daquan Yu is a Distinguished Professor of Xiamen University and the founder of Xiamen Sky Semiconductor Co., Ltd. He was the President of Research Academy of Advanced Packaging Technology of TSHT Group from 2014 to 2019. Before that, he was a professor of Institute of Microelectronics, Chinese Academy of Sciences from 2010 to 2015. He had carried out research work at Fraunhofer IZM in Germany, and Institute of Microelectronics in Singapore from 2005 to 2010. He has authored or co-authored more than 200 peer-reviewed technical publications and holds more than 70 patents. He is a member of the Expert Committee of the 02 National Science and Technology Major Program of China, vice president of MEMS branch of China Semiconductor Industry Association, and a senior member of IEEE.

ICEP 20th Anniversary Special Lectures

A Stacked Direct Time of Flight Depth Sensor for Automotive LiDAR with SPAD Pixels

Oichi Kumagai
Sony Semiconductor Solutions

In addition to sensing devices such as cameras and millimeter wave radar, LiDAR is becoming ever more important as a method of high-precision detection and recognition of not only road conditions but also the location and shape of objects such as vehicles and pedestrians. This trend is being driven by the popularization of advanced driver assistance systems (ADAS) and the need for this technology in autonomous driving (AD).

SPAD is a pixel structure that uses avalanche multiplication to amplify electrons from a single incident photon, causing a cascade like an avalanche, and it can detect even weak light. It is possible to accomplish long-distance, high-precision distance measuring by employing SPAD as the detector in a dToF sensor, which measures the distance to an object based on the time of flight (time difference) of a light emitted from a light source until it returns to the sensor, after being reflected by the object. Now, by leveraging Sony's technologies such as back-illuminated pixel structure, stacked configurations and Cu-Cu connections cultivated in the development of CMOS image sensors, and achieving the SPAD pixels and distance measuring processing circuitry on a single chip, Sony has succeeded in developing a compact yet high-resolution sensor. This enables high-precision, high-speed measurement at 15-centimeter range resolutions up to a distance of 300 meters. The new development will also help enable detection and recognition under severe conditions such as various temperature and weather as required for automotive equipment, thereby contributing to greater reliability for LiDAR. Achieving a single chip also helps lower the cost of LiDAR.

■ Biography

Oichi Kumagai joined Sony Corporation, Kanagawa, Japan, in 2007. He is a Senior Manager leading the time-of-flight depth sensors technology development activities in Automotive. He has over 10 years of experience in image sensor and has technical leadership in time-of-flight depth sensor, with a focus on single-photon detector and 3D imaging and ranging systems.

Present and Future of Semiconductor Technology in the Age of Paradigm Shift

Akihisa Sekiguchi
TOKYO ELECTRON

The year 2020 saw many changes in the way we conduct our lives. As we wrestled with the pandemic that still affects us, transformation took place in the way we work, study, travel and interact with each other in order to cope with the problem. This transformation was enabled in large part by advances in semiconductor technology and ICT (information and communication technology) which took decades to create.

In the talk, the speaker will describe some of the transformation that has taken place (the paradigm shifts), provide an overview on the state of the industry`s process technology used to create essential devices (logic, memory) and talk about the extendibility of technology going forward.

Time permitting, the speaker will also comment on the future direction of computing.

■ Biography

- Dr. Akihisa (Aki) Sekiguchi currently serves as the Corporate Alliance Strategy GM and Deputy Division General Manager of Tokyo Electron Limited's Corporate Innovation Division.
- He is responsible for planning and executing worldwide alliance strategy for this corporate division and in previous roles he has led corporate marketing and R&D.
- He is on SEMI's Board of Industry Leaders, SEMI CTO Forum and also serves as a member of the Technology Advisory Board for New York Creates.
- Prior to joining Tokyo Electron in 2007, he worked for IBM Microelectronics Division for 17 years. As part of the Semiconductor Research and Development Center, he worked on development of FEOL, MOL, and BEOL process technologies that enabled IBM's DRAM and SOI based logic technologies.
- During his last three years with IBM, he was responsible for process technology transfer from IBM to Sony that enabled Play Station 3.
- Aki earned his Ph.D. in Applied Physics from Columbia University, M. Eng. and B.S. in Engineering Physics from Cornell University, and a MBA in Finance from Stern School of Business (NYU while working for IBM). His doctoral thesis was on experimental plasma physics for fusion.

Room A

8:45 – 9:00 **Opening Remark**

9:00 – 10:00 **Keynote Lecture I:** Comprehensive SiP Enabling New System Integration
CP Hung, ASE Group
Chairs: Y. Orii, Nagase, S. Hayashida, ASE Group

10:00 – 10:10 **Break**

Room A	Room B	Room C
WA1: Heterogeneous Integration Roadmap-1 Chairs: Y. Orii, Nagase, S. Aoki, Lintec **WA1-1 <Session Invited>** HIR Overview Wilmer R Bottoms, 3MT Solutions / USA **WA1-2 <Session Invited>** Beyond Scaling - Trends in AI Hardware R&D Dale McHerron, IBM Research / USA **WA1-3 <Session Invited>** Organic Interposer (CoWoS-R) Technology Shin-Puu Jeng, TSMC / Taiwan **WA1-4 <Session Invited>** Advanced Packaging : Road Mapping the Future Ravi Vithal Mahajan, Intel / USA	**WB1: Interconnections-1** Chairs: M. Fujino, AIST, H. Ohkuma, HTO **WB1-1** Pressureless and Low Temperature Direct Bonding on Si, SiC and GaN via Ag Paste Sinter-joining Zheng Zhang, Chuantong Chen, Aiji Suetake, Ming-Chun Hsieh, Aya Iwaki, Katsuaki Suganuma, Osaka University / Japan **WB1-2** Cobalt-Tin Intermetallic Compounds as Alternative Surface Finish for Low Temperature Die-to-Wafer Solder Stacking Fumihiro Inoue, Jaber Derakhshandeh, Carine Gerets, Eric Beyne, imec / Belgium **WB1-3** Photonic Sintering of Composite Pastes with Copper Oxide Powders Using Different Light Sources Wei-Han Cheng[1], Po-Hsiang Chiu[1], Yan-Jie Li[1], Ming-Tsang Lee[2], Kiyokazu Yasuda[3], Jenn-Ming Song[1,3], [1]National Chung Hsing University, [2]National Tsing Hua University / Taiwan, [3]Osaka University / Japan (11:25)	**WC1: Emerging Technologies-1** Chairs: N. Fujimori, Olympus Medical Systems, T. Kasahara, Hosei University **WC1-1** Fabrication of Micropatterned Fish Scale Collagen Scaffold Using Soft Lithography for Oral Mucosa Tissue Engineering Kazuma Kishimoto[1], Keito Miwa[1], Ayako Suzuki[2], Isamu Yamaguchi[3], Yoshihiro Kodama[3], Orakarn Suebsamarn[2], Shuichi Shoji[1], Kenji Izumi[2], Jun Mizuno[1,4], [1]Waseda University, [2]Niigata University, [3]Taki Chemical, [4]Suwa University of Science / Japan **WC1-2** Battery Less Soil Moisture Sensors for Strawberry Seedlings Haruichi Kanaya[1], Osamu Takiguchi[2], Shunsuke Uto[3], Katsumi Shimomura[3], [1]Kyushu University, [2]ALSENS, [3]Fukuoka Agriculture and Forestry Research Center / Japan **WC1-3** Ni coated Cu Foils as the Substrate for Flexible Piezocomposite Power Generators Chi-Hsuan Lin[1], Jun-Hao Lee[1], Chia-Che Wu[2], Jenn-Ming Song[1], [1]National Chung Hsing University, [2]National Chung Hsing University / Taiwan **WC1-4** MCU and Motor Driver Leaf Modules of Coin-Sized PCBs in an Open-Innovation IoT/CPS Platform Kenichi Agawa[1], Tokihiko Mori[2], Ryoji Ninomiya[1], Minoru Takizawa[1], Takayasu Sakurai[2], [1]Toshiba Electronic Devices & Storage, [2]The University of Tokyo / Japan

11:50 – 12:40 **Lunch Time**

Room A

12:40 – 13:40 **Keynote Lecture II:** Future View: technology merger strengthens evolution of semiconductor chips in the hyper-scaling AI/ML era
Kazuya Okamoto, Yamaguchi University / Osaka University
Chairs: A. Shigetou, NIMS, Y. Kanechika, Tokuyama

13:40 – 13:50 **Break**

Room A	Room B	Room C
WA2: Heterogeneous Integration Roadmap-2 Chair: Y. Orii, Nagase **WA2-1 <Session Invited>** Introduction to HIR Workshop Session William Chen, ASE / USA (14:00) **WA2-2 <Session Invited>** Heterogenous Integration for HPC and Data Centers Kanad Ghose, SUNY-Binghamton, Dale Becker, IBM / USA (14:20) **WA2-3 <Session Invited>** Photonics TWG update Amr S Helmy, University of Toronto / Canada (14:40) **WA2-4 <Session Invited>** Wafer Level and Panel Level Packaging John Hunt, ASE / USA (15:00) **WA2-5 <Session Invited>** Overview of the Co-Design Chapter Jose Schutt Aine, University of Illonois / USA (15:20) **WA2-6 <Session Invited>** HIR Workshop Session Wrap-up Tom Salmon, SEMI / USA	**WB2: Interconnections-2** Chairs: K. Yasuda, Osaka University, K. Hirano, Panasonic **WB2-1** Reliable Joint Material by Sn-Cu-Ni IMC Fine Particles Shigenobu Sekine[1], Hiroaki Ikeda[1], Shigeo Arai[2], [1]Napra, [2]Nagoya University / Japan **WB2-2** A Technique to Mount Narrow-Pitch Micro Solder Balls Shunichi Haraguchi[1], Chisato Oyama[1], Kotaro Usuda[2], Hideki Ikeda[1], [1]KOMORI, [2]SERIA ENGINEERING / Japan **WB2-3** Voidless Chip-on-Wafer Process for Functional Interposer Yoshiaki Satake[1,2], Tatsuya Funaki[1,2], Kyosuke Kobinata[1,3], Youngsuk Kim[1,3], Takayuki Ohba[1], [1]Tokyo Institute of Technology, [2]Murata Manufacturing, [3]DISCO / Japan (15:05)	**WC2: Emerging Technologies-2** Chairs: N. Fujimori, Olympus Medical Systems, T. Nonaka, Huawei Technologies Japan **WC2-1 <Session Invited>** Industry 4.0 Adoption: A Journey in Smart Supply Chain and Manufacturing Transformation Feng Xue, IBM / Singapore **WC2-2** Development of Power Management System for RF Energy Harvester Masaya Murakami[1], Mohamed M. Mansour[2], Shota Torigoe[2], Shuya Yamamoto[2], Haruichi Kanaya[2], [1]SEIKO ELECTRIC, [2]Kyushu University / Japan **WC2-3** Silicon-Photonics-Embedded Interposers and Their Applications Koichi Takemura[1], Daisuke Ohshima[1], Akihiro Noriki[1,2], Daisuke Okamoto[1], Akio Ukita[1], Jun Ushida[1], Masatoshi Tokushima[1], Daisuke Shimura[1], Tsuyoshi Aoki[1], Takeru Amano[1,2], [1]Photonics Electronics Technology Research Association, [2]National Institute of Advanced Industrial Science and Technology / Japan **WC2-4** A High-Sensitivity Olfactory System with a Graphene FET Biosensor and a Portable Odorant Capture Module Hideyuki Tomizawa[1], Kou Yamada[1], Hiroshi Hamasaki[1], Yoshiaki Sugizaki[1], Miyuki Tabata[2], Yuji Miyahara[2], Atsunobu Isobayashi[1], [1]Toshiba, [2]Tokyo Medical and Dental University / Japan

15:30 – 15:40 **Break**

WA3: Thermal Management Chairs: H. Sakamoto, Huawei Technologies Japan, T. Hatakeyama, Toyama Prefectural University **WA3-1 <Session Invited>** Possibility of Next Innovation of Forced Convection Cooling in High-Density Packaging Electronic Equipment by Pulsating Flow Phenomena from Knowledge of Nature Takashi Fukue, Kanazawa Institute of Technology / Japan **WA3-2** Low Pressure Subcooled Boiling in a Compact Vessel for Cooling Technology Noriyuki Unno, Kazuhisa Yuki, Risako Kibushi, Koichi Suzuki, Sanyo-Onoda City University / Japan **WA3-3** Parameter Identification of Distributed Thermal Network for Surface Mount Type Power Semiconductor Packages Koji Nishi, Ashikaga University / Japan **WA3-4** Room-Temperature Bonding of AlN Ceramic and Si Semiconductor Substrates for Improved Thermal Management Takashi Matsumae[1], Yuichi Kurashima[1], Hideki Takagi, Kazunori Nishizono[2], Tsutomu Amano[2], Eiji Higurashi[1], [1]National Institute of Advanced Industrial Science and Technology, [2]MARUWA / Japan	**WB3: Interconnections-3** Chairs: T. Aoki, IBM Japan, Y. Morikawa, Ulvac **WB3-1** Low Temperature Bonding of Cu Bump to WBG Device Using the Surface Activation Method Tadatomo Suga[1], Kai Takeuchi[1], Seongbin Shin[1], Nora Martinez[1], Yoshinari Ikeda[2], Akira Hirao[2], Motohito Hori[2], [1]Meisei University, [2]Fuji Electric / Japan **WB3-2** Surface Activated Bonding of Nb-Nb for Surperconducting Device Interconnect Yuta Takahashi[1,2], Masahisa Fujino[2], Takashi Matsumae[2], Hiroshi Nakagawa[2], Katsuya Kikuchi[2], Tohru Taino[1], [1]Saitama University, [2]National Institute of Advanced Industrial Science and Technology / Japan **WB3-3** Effects of Surface Physical Properties on Ultrasonic Cu/Cu Bonding I-You Yu, Liang-Shing Shih, Jenn-Ming Song, National Chung Hsing University / Taiwan (16:55)	**WC3: Power Electronics** Chairs: Y. Inaba, Denso, T. Onishi, Grand Joint Technology **WC3-1** Packaging of (650 V, 150 A) GaN HEMT with Low Parasitics and High Thermal Performance Shengchang Lu, Tianyu Zhao, Rolando Burgos, Guo-Quan Lu, Virginia Tech / USA **WC3-2** Direct Bonding of Diamond and Si Substrates Using NH_3/H_2O_2 Cleaning Shoya Fukumoto[1,2], Takashi Matsumae[2], Yuichi Kurashima[2], Hideki Takagi[2], Hitoshi Umezawa[2], Masanori Hayase[1], Eiji Higurashi[2], [1]Tokyo University of Science, [2]National Institute of Advanced Industrial Science and Technology / Japan **WC3-3** Low Temperature Bonding of GaN and Carbon Composite via Au Capping Layer Activated by Ar Fast Atom Bombardment Kai Takeuchi[1], Suga Tadatomo[1], Atsushi Tanaka[2], Akio Wakejima[3], [1]Meisei University, [2]Nagoya University, [3]Nagoya Institute of Technology / Japan (16:55)

15:40 – 17:20

	Room A	Room B	Room C
9:00 10:00	~~**Keynote Lecture III:** Direct Bonding: A New Paradigm Shift in Semiconductor Assembly~~ **(Cancelled)** ~~Belgacem Haba, Xperi~~ Chairs: O. Suzuki, Namics, N. Tanaka, Showadenko Materials		
10:00 10:10	**Break**		
10:10 11:50	**TA1: iNEMI Session** Chairs: Y. Tomita, Intel, H. Yamada, Toshiba **TA1-1 <Session Invited>** 5G Standard Reference Materials Nathan Orloff, National Institute of Standards and Technology / USA **TA1-2** Predictive Modelling Methodologies for Bi-Material Wafer Warpage Kang Eu Ong[1], Wei Keat Loh[1], Jenn An Wang[2], Arvind Purushotaman[3], Tatsuro Yoshida[4], Kei Murayama[4], Makoto Tsukahara[4], Ron W. Kulterman[5], Haley Fu[6], [1]Intel Technology / Malaysia, [2]CoreTech System (Moldex3D) / Taiwan, [3]ANSYS / USA, [4]Shinko Electric Industries / Japan, [5]Flex / USA, [6]iNEMI / China **TA1-3** Voids Inspection Capability Study in First-Level Interconnects for Flip Chip Packages Masahiro Tsuriya[1], Kor Oon Lee[2], Kiyoshi Oi[3], Sze Pei Lim[4], Yvonne Yeo[5], Keith Sweatman[6], Toshiaki Ono[7], Kei Murayama[3], Steven R. Martell[7], Haruo Shimamoto[8], Evstatin Krastev[7], [1]iNEMI / Japan, [2]Intel / Malaysia, [3]Shinko Electric Industries / Japan, [4]Indium / Malaysia, [5]IBM / Singapore, [6]Nihon Superior / Australia, [7]Nordson Electronics Solutions / Japan & USA, [8]AIST, Japan **TA1-4** Low Temperature 1st Level Interconnect in Packaging and Its Challenges Sze Pei Lim[1], Charles Arvin[2], David Locker[3], Ravi Pokhrel[4], Wei Keat Loh[5], Keith Sweatman[6], Derek Daily[7], Naoki Kubota[8], Masahiro Tsuriya[9], [1]Indium / Malaysia, [2]IBM, [3]DoD, [4]Dupont / USA, [5]Intel / Malaysia, [6]Nihon Superior / Australia, [7]Senju Metal Industry / USA, [8]Tamura, [9]iNEMI / Japan	**TB1: Materials and Processing-1** Chairs: S. Takyu, Lintec, H. Hozoji, AIST **TB1-1 <Session Invited>** Advanced Thermal Materials and Systems: Technology and Trend Analysis for the Future Yukihiro Kanechika, Kazuya Okamoto, Yamaguchi University / Japan **TB1-2** Characterization of Additively Formed Copper Layer by Blue Laser-Sintered Copper Nanoparticles Kiyokazu Yasuda[1], Yuki Takada[1], Jenn-Ming Song[1,2], [1]Osaka University / Japan, [2]National Chung Hsing University / Taiwan **TB1-3** Die-attach Properties of Pressure-sintered Copper Joints on Adhesive Metallization Surfaces in N_2 Atmosphere Dai Ishikawa[1], Bao Ngoc An[2], Matthias Mail[2], Helge Wurst[2], Benjamin Leyrer[2], Thomas Blank[2], Marc Weber[2], Hideo Nakako[1], [1]Showa Denko Materials / Japan, [2]Karlsruhe Institute of Technology / Germany **TB1-4** Fine Pitch Bumping and Flip Chip Joining with Sn-Bi Based Solders by Injection Molded Solder Technology Toyohiro Aoki[1], Katsuhiro Yoshida[2], Koki Nakamura[2], Takashi Hisada[1], Kozo Fujimoto[2], Shinji Fukumoto[2], [1]IBM Japan, [2]Osaka University / Japan	**TC1: Advanced Interface** Chairs: J. Mizuno, Waseda University, T. Matsunaga, Tottori University **TC1-1 <Session Invited>** Hybrid Bonding Without Vacuum and High Temperature for Cross-Cutting Applications Akitsu Shigetou, National Institute for Materials Science / Japan **TC1-2 <Session Invited>** Metasurface Quantum-Well Infrared Photodetectors Hideki T. Miyazaki, National Institute for Materials Science / Japan **TC1-3 <Session Invited>** High-Performance SAW Devices Using Bonded Dissimilar-Material Structures Shoji Kakio, University of Yamanashi / Japan **TC1-4 <Session Invited>** Fabrication and Characterization of Microfluidic Electrogenerated Chemiluminescence Devices Takashi Kasahara[1], Jun Mizuno[2], [1]Hosei University, [2]Waseda University / Japan
11:50 12:40	**Lunch Time**		
12:40 13:40	**Poster Session**		
13:40 13:50	**Break**		
13:50 15:30	**TA2: LED Technologies** Chairs: K. Ichikawa, Nichia, A. Okuno, Green Planets **TA2-1 <Session Invited>** Medical Study of 400-410nm LED and micro LED Atsushi Okuno, Green Planets / Japan **TA2-2 <Session Invited>** 2MGy High Radiation Tolerance LED & UVC LED Packaging Tetsuya Onishi, Grand Joint Technology / Hong Kong **TA2-3 <Session Invited>** Ultrafast Laser Transfer Technology Yoshiyuki Arai, Toray Engineering / Japan **TA2-4 <Session Invited>** Fluidic Assembly of microLED Displays Paul Schuele, eLux / USA	**TB2: Materials and Processing-2** Chairs: Y. Kanechika, Tokuyama, K. Shibayama, Sekisui Chemical **TB2-1** Effect of Sequential Plasma Activation on Al_2O_3 for Low Temperature Bonding of Glass Kai Takeuchi, Tadatomo Suga, Meisei University / Japan **TB2-2** Low-temperature Printable and Stretchable Circuit Board and Its Application to Flexible Hybrid Electronics Teppei Araki[1,2], Yusuke Okabe[3], Naoko Kurihira[1], Yuko Kasai[1,2], Yuki Noda[1], Tsuyoshi Sekitani[1,2], [1]Osaka University, [2]AIST-Osaka University, [3]CEMEDINE / Japam **TB2-3** X-ray Radiolysis-Induced-Photochemical Reaction at Interface Between Liquid and Substrate S. Saegusa[1], N. Akamatsu[1], I. Sakurai[2], I. Okada[3], Y. Utsumi[1], A. Yamaguchi[1], [1]University of Hyogo, [2]Nagoya University, [3]Aichi Synchrotron Radiation Center / Japan **TB2-4** Analysis of Low Friction Force and Low Contact Resistance Film Using Sn-Cu Plating Hiroki Hayashi[1,2], Naohiro Takaine[1], Hiroyuki Funasaki[1], Mitsuhiro Watanabe[2], [1]TAKAMATSU Plating, [2]Kanto Gakuin University / Japan	**TC2: Quality, Modeling, and Reliability** Chairs: K. Yasuda, Osaka University, H. Sakamoto, Huawei Technologies Japan **TC2-1** Characterization Of Copper Sintered Interconnects By Transient Thermal Analysis Maximilian Schmid, Sri Krishna Bhogaraju, Gordon Elger, Technische Hochschule Ingolstadt / Germany **TC2-2** Crevice Elimination and Stitch Integrity Improvement on eaded Packages Thru Shifted Lead Neck Design Dolores B. Milo, Gloria B. Manaois, Texas Instruments Philippines / Philippines **TC2-3** Study on Suppression of External Stress Type Tin Whisker by PR Current Method Hiroyuki Iwamoto[1], Katsuji Nakamura[1], Kaichi Tsuruta[1], Osamu Munekata[2], [1]Senju Metal Industry, [2]Industrial Analysis Service / Japan (15:05)
15:30 15:40	**Break**		
15:40 16:55	**TA3: IMPACT Session** Chairs: J. Mizuno, Waseda University, A. Shigetou, NIMS **TA3-1 <Session Invited>** Shear Behavior of the High Temperature Pb-Free Solder Joint with Zn-25Sn-xTi-yCu Kwang-Lung Lin, Che-Wei Chang, Min-Ren Chen, National Cheng Kung University / Taiwan **TA3-2 <Session Invited>** Advanced SiP Development for mmWave Antenna in Package Yupo Wang, Siliconware Precision Industries / Taiwan **TA3-3 <Session Invited>** Reliability Issues of Cu-Cu Direct Bonds Chih Chen[1], Kai-Cheng Shie[1], Po-Ning Hsu[1], King-Ning Tu[1,2], [1]National Yang Ming Chiao Tung University / Taiwan, [2]UCLA / USA United	**TB3: Advanced Packaging** Chairs: T. Aoki, IBM Japan, M. Aoyagi, AIST **TB3-1 <Session Invited>** Highlighting a New Package!! "PhotoMold" Shuzo Akejima, Rising Technologies / Japan **TB3-2** New Ag Pastes Siter Joining on Ag and Cu Surface for High Temperature Application Jinting Jiu, Yoshie Tachibana, Shunsuke Koga, Ryuki Horie, Tomoki Sasaki, Senju metal Industry / Japan **TB3-3** Development of Au/Pt/Ti Multilayers for Wafer-Level Packaging and Residual Gas Gettering Shingo Kariya[1], Takashi Matsumae[2], Yuichi Kurashima[2], Hideki Takagi[2], Masanori Hayase[1], Eiji Higurashi[2], [1]Tokyo University of Science, [2]National Institute of Advanced Industrial Science and Technology / Japan	

	Room A	Room B	Room C
9:00 10:00	**Keynote Lecture IV:** Superconducting Circuits for Quantum Technologies Yasunobu Nakamura, The University of Tokyo / RIKEN Center for Emergent Matter Science Chairs: M. Fujino, AIST, S. Takyu, Lintec		
10:00 10:10	**Break**		
10:10 11:50	**FA1: Quantum Computing / Annealer** Chair: M. Fujino, AIST, Y. Tabuchi, RIKEN **FA1-1 <Session Invited>** Digital Annealer and Its Applications Taisuke Iwai, Fujitsu / Japan **FA1-2 <Session Invited>** Overview and Present Status of CMOS Annealing Masanao Yamaoka, Hitachi / Japan **FA1-3 <Session Invited>** Quantum Annealer Using Superconducting Parametric Oscillators Tsuyoshi Yamamoto, NEC / Japan **FA1-4 <Session Invited>** Combinatorial Optimization Machines Using Quantum or Classical Parametric Oscillators Hayato Goto, Toshiba / Japan	**FB1: Epoxy in Innovation** Chairs: M. Oda, Printed Electronics Network, M. Inoue, Gunma University **FB1-1** Development of Flexible Epoxy Film with High Thermal Stability, Especially Suitable for Display and Printed Electronics Applications Iori Doi, Takashi Komori, Noriyasu Yamane, Kotaro Nozawa, Takayoshi Hirai, Mitsubishi Chemical / Japan **FB1-2** Development of Stretchable Epoxy Film with High Thermal Stability, Especially Suitable for Printed Electronics Applications Iori Doi, Takashi Komori, Noriyasu Yamane, Kotaro Nozawa, Takayoshi Hirai, Mitsubishi Chemical / Japan **FB1-3 <Session Invited>** Fabrication of Stretchable Electrode with Epoxy Film using Printing Technology Tomohito Sekine[1], Kosuke Muraki[1], Itaru Watanabe[2], Iori Doi[2], Noriyasu Yamane[2], Shizuo Tokito[1], [1]Yamagata University, [2]Mitsubishi Chemical / Japan **FB1-4** Development of Novel Low Dielectric Epoxy Resin for High Frequency Applications Takaaki Watanabe, Noriyuki Kida, Makoto Takahashi, Takayoshi Hirai, Mitsubishi Chemical / Japan	**FC1: High-Speed, Wireless & Components** Chairs: K. Yamada, Toshiba, K. Hasegawa, JSR **FC1-1 <Session Invited>** Wired and Wireless Seamless Networks for Beyond 5G Tetsuya Kawanishi, Waseda University / Japan **FC1-2** Prototype Evaluation of Antennas with Artificial Magnetic Conductor for Firefighter Support Systems Yusuke Ikuma[1], Takahiko Yamamoto[1], Masayuki Mizuno[1], Yoshifumi Ohmiya[1], Kohji Koshiji[1], Yuji Shimizu[2], Tetsuya Shimizu[2], [1]Tokyo University of Science, [2]Tokyo Fire Department / Japan **FC1-3** Impact of Modularization on the Design Process -Case Study of Antenna Design for Smartphones- Atsushi Maeda, Hirofumi Tatsumoto, University of Tsukuba / Japan (11:25)
11:50 12:40	**Lunch Time**		
12:40 13:40	**Poster Session**		
13:40 13:50	**Break**		
13:50 14:50	**Keynote Lecture V:** Progress of Wafer Level Packaging Technology for RF Devices at 5G Era Daquan Yu, Xiamen University Chairs: E. Higurashi, AIST, S. Takyu, Lintec		
14:50 15:00	**Break**		
15:00 17:10	**ICEP 20th Anniversary Special Lecture: Challenges and Future Directions in the Semiconductor Industry** A Stacked Direct Time of Flight Depth Sensor for Automotive LiDAR with SPAD Pixels Oichi Kumagai, Sony Semiconductor Solutions Present and Future of Semiconductor Technology in the Age of Paradigm Shift Akihisa Sekiguchi, Tokyo Electron Chairs: T. Ohba, Tokyo Institute of Technology, E. Higurashi, AIST		
17:10 17:20	**Introduction of ICEP 2022** **Closing Remark**		

Poster Session

From 12:40-14:40 on May 13 (P01-P07 and Sponsors)

P01 Development of Semi-Analytical Formulation for Asymmetric Warpage Prediction in Fan-out Reconstitution Process
K.-S. Chen[1], Y. -C. Lee[1], C. -Y. Chen[1], T. -Y. Chen[2], D. -L. Chen[2], David Tarng[2], [1]National Cheng-Kung University, [2]Advanced Semiconductor Engineering / Taiwan

P02 The Simulation and Detection of Copper/Polyimide Delamination of Fan-Out Package Trace/ Passivation Interface
Chung-Yu Ke, Liang-Pin Chen, Siliconware Precision Industries / Taiwan

P03 Analysis of Stress Generated Interface of Trench MIM (Metal-Insulator-Metal) Capacitor Structure
Eunsol Jo, Jung-Rae Park, Cheong-Ha Jung, Gu-Sung Kim, Electronic Package Research Center / Korea

P04 Evaluation of Dispersibility of Silver Nanoparticle Ink by TEM and NMR
Hirotaka Shioji[1], Kazuo Kimura[1], Shin Inamoto[1], Naoki Muraki[1] Daisuke Kumaki[2], Shizuo Tokito[2], [1]Toray Research Center, [2]Yamagata University / Japan

P05 Superhydrophobic Surface Based on Silane Coating on Silicon-Based Electrospun Nanostructures
Cho-Liang Chung, ChunWei Cheng, Cheng-Ying Tsai, Yu-Ching Chao, Wei-Hao Chen, I-Shou University / Taiwan

P06 Effects of Moisture and Oxygen on the Morphology Evolution of Electrospinning Woven
Sian-Sheng Li, Huai-You Lee, Yi-Min Lin, Cho-Liang Chung, I-Shou University / Taiwan

P07 Accuracy Assessment of Quantification Method of Cellulose Nano-Fiber in Nickel Plating Film Using Image Analysis
Makoto Iioka, Ikuo Shohji, Tatsuya Kobayashi,, Gunma University / Japan

Sponsor Zuken

Sponsor Fujitsu Interconnect Technologies

Sponsor Global Net

Sponsor Bondtech

From 12:40-13:40 on May 14 (P08-P14 and Sponsors)

P08 Materials Informatics Technology for Using Eco-Friendly Materials
Tomio Iwasaki, Hitachi / Japan

P09 Analysis of Interfacial Conductivity Variations of Copper-Filled Electrically Conductive Adhesives During Environmental Tests
Daisuke Otajima, Yuki Saito, Masahiro Inoue, Gunma University / Japan

P10 Structural Control of PEDOT: PSS Thin Films Using Non-Ionic Surfactants for Enhancing Stretchability
Kaito Oozutsumi, Masahiro Inoue, Gunma University / Japan

P11 Analysis of Reflection Characteristics and Radiation Efficiency on Thickness and Conductivity of Monopole Antenna Using Transparent Conductive Film
Yuri Yamada[1], Fukuro Koshiji[1], Yoji Yasuda[1], Takayuki Uchida[1], Katsumi Yamada[1], Kohji Koshiji[2], [1]Tokyo Polytechnic University, [2]Tokyo University of Science / Japan

P12 Investigation of Broadband Circularly-Polarized Unbalanced Dipole Antenna Consisting of Semicircular and Trapezoidal Elements
Hironori Takahashi [1], Fukuro Koshiji[1], Kohji Koshiji[2], [1]Tokyo Polytechnic University, [2]Tokyo University of Science / Japan

P13 Via Resonance Amplitude Control
Vinod Arjun Huddar, Rambus / India

P14 Development of Novel BN Filler for High Thermal Conductivity Packaging Material
Shota Daiki, Kyoichi Fujinami, Seiji Imazumi, Saiko Fujii, Isao Masada, Yukihiro Kanechika, Teruhiko Nawata, Masahide Ueda, Tokuyama Corporation / Japan

Sponsor Namics

Sponsor Huawei Technologies Japan

Sponsor Toray

Sponsor TDC

On-Demand Session (Streaming Period: May 12-25)

OD1: Advanced Packaging

OD1-1
Develpoment of Leadframe for Quad Flat No-lead Package
Mei-Ling Wu, Che-Wei Kang, National Sun Yat-sen University / Taiwan

OD1-2
Evaluation of Direct Metallization Technology Plating Properties with Excellent Material Selectivity
Takuya Komeda, Tetsuji Ishida, Hisamitsu Yamamoto, C. Uyemura / Japan

OD1-3
Development of High Reliablity Joint of Sn-Bi Solder for 2.3D Organic Package
Shota Miki, Koyuki Kawakami, Kei Murayama, Kiyoshi Oi, SHINKO ELECTRIC INDUSTRIES / Japan

OD1-4
Mechanical Reliability Analysis of Dual Side Molding SiP Module
Tse-Wei Liao, Wei-Hong Lai, Hsin-Chih Shih, Dao-Long Chen, David Tarng, CP Hung, Advanced Semiconductor Engineering / Taiwan

OD1-5
Copper sintered Si3N4 Power Modules in Thermal Shock Tests
Thomas Blank[1], Hongpeng Zhang[1], Helge Wurst[1], Benjamin Leyrer[1], Felix Steiner[1], Dai Ishikawa[2], Udo Geckele[1], Ivan Peric[1], [1]Karlsruhe Institute of Technology / Germany, [2]Showa Denko Materials / Japan

OD1-6
Low Temperature Bonding with Wafer Level Nanocrystalline Cu Film
Wei-Lan Chiu, Chia-Wen Chiang, Hsiang-Hung Chang, Industrial Technology Research Institute / Taiwan

OD1-7
Novel Approach of Die Attach Technology for SiC Power Module by Pure Al Thin Film Bonding
Chuantong Chen, Katsuaki Suganuma, Osaka University / Japan

OD1-8
Prediction of Fan-Out Level Packaging Warpage Using PSO-based Modified Convolutional Neural Network Model with Laplacian Filter
G. R. Huang, M. Y. Chen, K. N. Chiang, National Tsing Hua University / Taiwan

OD1-9
Electromigration Improvement by Graphene on Cu Wire for Next Generation VLSI
Y. T. Hung[1], J. Z. Huang[1,2], H. H. Chang[1], K. P. Huang[1], O. H. Lee[1], W. L. Chiu[1], H. J. Jian[1], K. C. Huang[1], W. C. Lo[1], J. S. Hu[1], C. I. Wu[1,2], [1]Industrial Technology Research Institute, [2]National Taiwan University / Taiwan

OD1-10
A Study of Factors Affecting Process-induced Warpage Behavior of Flip Chip Package on Package
Yi-Huang Chen, Ling-Ching Tai, Yan-Cheng Liu, Hsien-Chie Cheng, Feng Chia University / Taiwan

TB3-3 (Pre-recorded video for live session presentation)
Development of Au/Pt/Ti Multilayers for Wafer-Level Packaging and Residual Gas Gettering
Shingo Kariya[1], Takashi Matsumae[2], Yuichi Kurashima[2], Hideki Takagi[2], Masanori Hayase[1], Eiji Higurashi[2], [1]Tokyo University of Science, [2]National Institute of Advanced Industrial Science and Technology / Japan

OD2: Quality, Modeling, and Reliability

OD2-1
Experimental Investigation of Ultra-Thin ilicon Wafers Warpage
Mei Ling Wu, Tzu Chi Tseng, National Sun Yat-sen University / Taiwan

OD2-2
Study of Substrate Materials on Bias-HAST Reliability of Fine Pitch FCBGA Package
Yu-Cheng Pai, Wen-Yu Teng, Hsuan-Hao Mi, Liang-Yih Hung, Andrew Kang, Yu-Po Wang, Siliconware Precision Industries / Taiwan

OD2-3
Prognostic Health Monitoring Method For Thermal Fatigue Failure Of Power Module Solder Joints Using The Grain Boundary Sliding Model
Hideaki Uehara, Tomoko Monda, Akira Kano, Tomoya Fumikura, Kenji Hirohata, Toshiba / Japan

OD2-4
White X-ray Nanodiffraction Study of Allotropic Phase Transformation of Hexagonal- into Monoclinic-Cu_6Sn_5
Pei-Tzu Lee[1], Wan-Zhen Hsieh[2], Cheng-Yu Lee[3], C. R. Kao[1], Cheng-En Ho[3], [1]National Taiwan University, [2]National Synchrotron Radiation Research Center, Taiwan, [3]Yuan Ze University / Taiwan

OD2-5
The Voids Growth Path on Sn-Ag Thin Film Under High Current Density
Zhi Jin[1], Yu-An Shen[1], Yang Zuo[2], S.H. Mannan[2], Hiroshi Nishikawa[1], [1]Osaka University / Japan, [2]King's College London / UK

OD2-6
Detection Of Die Attach Defects Through Rapid Thermal Transient Tests
Voon Hon Wong[1], Andras Vass-Varnai[2], Antonio Caruso[3], Tomoaki Hara[4], Alvin Hsu[5], Gang Wang[5], [1]Siemens Digital Industry Software / Singapore, [2]Siemens Digital Industry Software / USA, [3]Siemens Digital Industry Software / Italy, [4]Siemens Digital Industry Software / Japan, [5]Siemens Digital Industry Software / Greater China

OD2-7
Detectable Resistance Increase of Open Defects in Assembled PCBs by Quiescent Currents Through Embedded Diodes
Yuya Okumoto[1], Hiroyuki Yotsuyanagi[1], Masaki Hashizume[1], Shyue-Kung Lu[2], [1]Tokushima University / Japan, [2]National Taiwan University of Science and Technology / Taiwan

OD3: Interconnections

OD3-1
Morphology and Mechanical Property of Cu Pillar Formed by Sintered Cu Nanoparticles for the Plating-Free Bumping Process
Chinami Marushima[1], Toyohiro Aoki[1], Sayuri Kohara[1], Ryota Yamaguchi[2], Nobuhiro Sekine[2], Kenichi Yatsugi[2], Kuniaki Sueoka[1], Takashi Hisada[1], [1]IBM Japan, [2]DIC / Japan

WB1-1 (Pre-recorded video for live session presentation)
Pressureless and Low Temperature Direct Bonding on Si, SiC and GaN via Ag Paste Sinter-joining
Zheng Zhang, Chuantong Chen, Aiji Suetake, Ming-Chun Hsieh, Aya Iwaki, Katsuaki Suganuma, Osaka University / Japan

WB2-1 (Pre-recorded video for live session presentation)
Reliable Joint Material by Sn-Cu-Ni IMC Fine Particles
Shigenobu Sekine[1], Hiroaki Ikeda[1], Shigeo Arai[2], [1]Napra, [2]Nagoya University / Japan

WB2-2 (Pre-recorded video for live session presentation)
A Technique to Mount Narrow-Pitch Micro Solder Balls
Shunichi Haraguchi[1], Chisato Oyama[1], Kotaro Usuda[2], Hideki Ikeda[1], [1]KOMORI, [2]SERIA ENGINEERING / Japan

OD4: Materials and Processing

OD4-1
Development of Novel Bevel Profile for Wafer-level Stacking Technology
Tatsuhiko Aoki[1,2], Manabu Hirasawa[2], Koji Izunome[2], Takayuki Ohba[1], [1]Tokyo Institute of Technology, [2]Global Wafers Japan / Japan

OD4-2
The Control of Material Surface Condition for Plasma Technology to Fabricate Advanced Packaging
Daisuke Hironiwa, Yasuhiro Morikawa, Tsuyoshi Kagami, Takashi Kurimoto, Kazumasa Horita, Ryuichiro Kamimura, ULVAC / Japan

OD4-3
High Aspect/Narrow Pitch Substrate Wiring and Bump Formation Using Imprinting Technology for Low Temperature Flip Chip Bonding
Hiroshi Komatsu[1], Daisuke Sakai[1], Nozomi Shimoishizaka[1], Toshihiro Yamada[2], [1]CONNECTEC JAPAN, [2]Industrial Research Institute of Niigata Prefecture / Japan

OD4-4
Novel Isotropic Low Dk/Df film for 5G Application
Meiten Koh1, Masayuki Shimura1, Shoya Sekiguchi2, Shoko Mishima2, Nobuhiro Ishikawa2, Toshiyuki Ogata2, 1Taiyo Ink MFG., 2Taiyo Holdings / Japan

OD4-5
Effects of Epoxy Molding Compound on Managed NAND(mNAND) Package Strain Enhancement
Joyce Chen[1], Vance Liu[1], Lewis Lin[1], Min Chung[1], Chong Leong, Gan[1], Hem Takiar[2], [1]Micron Technology / Taiwan, [2]Micron Technology / USA

OD4-6
Surface Modification of Tetra-needle like ZnO (T-ZnO) and Characterization of Interface Between Sn1.0Ag0.5Cu and NiO Decorated TZnO
Fupeng Huo[1], Keke Zhang[2], Hiroshi Nishikawa[1], [1]Osaka University / Japan, [2]Henan University of Science and Technology / China

OD4-7
Better Warpage Control by Using Low Temperature Solder for Large FCBGA Application
Da-Sheng Lai, Jackson Lee, Joe Huang, Yu-Po Wang, Siliconware Precision Industries / Taiwan

OD4-8
Post Mechanical Shock Test Failure Analysis on Mixed SnAgCu-BiSn BGA Solder Joints
Raiyo Aspandiar[1], Kei Murayama[2], Pubudu Goonetilleke[1], Jagadeesh Radhakrishnan[1], Haley Fu[3], [1]Intel / USA, [2]Shinko Electric Industries / Japan, [3]iNEMI / China

OD4-9
Effect of 4.0 mass % Cu Addition on Microstructure and Mechanical Properties of In-48Sn Alloy
Duy Le Han[1,2], Byungho Park[1], Hiroshi Nishikawa[1], [1]Osaka University / Japan, [2]Hanoi University of Science and Technology / Vietnam

OD4-10
High-Performance Film-Type Thermal Interface Material Containing Vertically Aligned Carbon Nanofibers
Wen-Yu Teng, Hsin-Ming Tseng, Liang-Yi Hung, Yu-Po Wang, Siliconware Precision Industries / Taiwan

OD4-11
Mechanism of Electrical Resistivity Variations of a Stretchable Wire Printed on Elastomer- Based Substrates During a Uniaxial Cyclic Tensile Test
Masahiro Inoue, Hikaru Watanabe, Kaito Oodutsumi, Gunma University / Japan

TB1-4 (Pre-recorded video for live session presentation)
Fine Pitch Bumping and Flip Chip Joining with Sn-Bi Based Solders by Injection Molded Solder Technology
Toyohiro Aoki[1], Katsuhiro Yoshida[2], Koki Nakamura[2], Takashi Hisada[1], Kozo Fujimoto[2], Shinji Fukumoto[2], [1]IBM Japan, [2]Osaka University / Japan

TB2-3 (Pre-recorded video for live session presentation)
X-ray Radiolysis-Induced-Photochemical Reaction at Interface Between Liquid and Substrate
S. Saegusa[1], N. Akamatsu[1], I. Sakurai[2], I. Okada[3], Y. Utsumi[1], A. Yamaguchi[1], [1]University of Hyogo, [2]Nagoya University, [3]Aichi Synchrotron Radiation Center / Japan

OD5: Emerging Technologies

OD5-1
Frequency Characteristics of Ultrathin and Transparent Organic Electrochemical Transistors with 1-μm-Thick Parylene Lamination
Kazuya Nishimura[1], Teppei Araki[1,2], Ashuya Takemoto[1,2], Mihoko Akiyama[1], Kazuki Kiriyama[1], Yuko Kasai[2], Naoko Kurihira[1], Takafumi Uemura[1,2], Tsuyoshi Sekitani[1,2], [1]Osaka University, [2]AIST-Osaka University / Japan

OD5-2
Electronic Band-Engineering of a Dumbbell-shaped Graphene Nanoribbon by the Application of Uniaxial Tensile Strain
Jowesh Avisheik Goundar, Qinqiang Zhang, Ken Suzuki, Hideo Miura, Tohoku University / Japan

OD5-3
Experimental Demonstration of Wireless Energy Harvesting for ZigBee Wireless Communication
Mohamed M. Mansour[1,3], Masaya Murakami[2], Shota Torigoe[1], Shuya Yamamoto[1], Haruichi Kanaya[1], [1]Kyushu University, [2]SEIKO ELECTRIC / Japan, [3]Electronics Research Institute / Egypt

WC1-2 (Pre-recorded video for live session presentation)
Battery Less Soil Moisture Sensors for Strawberry Seedlings
Haruichi Kanaya[1], Osamu Takiguchi[2], Shunsuke Uto[3], Katsumi Shimomura[3], [1]Kyushu University, [2]ALSENS, [3]Fukuoka Agriculture and Forestry Research Center / Japan

WC2-2 (Pre-recorded video for live session presentation)
Development of Power Management System for RF Energy Harvester
Masaya Murakami[1], Mohamed M. Mansour[2], Shota Torigoe[2], Shuya Yamamoto[2], Haruichi Kanaya[2], [1]SEIKO ELECTRIC, [2]Kyushu University / Japan

OD6: High-Speed, Wireless & Components

OD6-1
Silver-Seed Cu-Wirings for High-Speed Transmission
Norimasa, Fukazawa, Wataru Fujikawa, Akinori Furutani, Shota Niibayashi, Hiroyuki Hagiwara, Jun Shirakami, DIC / Japan

OD7: Optoelectronics

OD7-1
Realizing Low Optical Crosstalk, Wide Color Gamut Mini-LED Displays via Laser-Patterned Quantum Dots Color Conversion Layer
Yuanjie Cheng, Jeffery C. C. Lo, Xing Qiu, S. W. Ricky Lee, Hong Kong University of Science & Technology / Hong Kong

OD8: Power Electronics

OD8-1
Effect of Sintering Density on Thermal Reliability by Non-Pressure Sintering Die-Attach
Ryo Kato, Masatoshi Okuda, Suguru Hashidate, Takamichi Mori, Junichiro Minami, Tetsuo Sakurai, Taro Fukui, OSAKA SODA / Japan

OD8-2
Design Optimization of Copper Patterns and Location of Power Semiconductors and Terminals
Yusuke Abe[1], Akira Hirao[2], Ryoichi Kato[2], Yoshinari Ikeda[2], Victor Parque[1], Muhammad Khairi Faiz[1], Makoto Yoshida[1], Tomoyuki Miyashita[1], [1]Waseda University, [2]Fuji Electric / Japan

OD8-3
The Effect of Solid-state Nanoporous Cu Bonding for Power Device
Byungho Park[1], Duy le Han[1,3], Mikiko Saito[2], Jun Mizuno[2], Hiroshi Nishikawa[1], [1]Osaka University, [2]Waseda University / Japan, [3]Hanoi University of Science and Technology / Vietnam

WC3-1 (Pre-recorded video for live session presentation)
Packaging of (650 V, 150 A) GaN HEMT with Low Parasitics and High Thermal Performance
Shengchang Lu, Tianyu Zhao, Rolando Burgos, Guo-Quan Lu, Virginia Tech / USA

WA3-2 (Pre-recorded video for live session presentation)
Low Pressure Subcooled Boiling in a Compact Vessel for Cooling Technology
Noriyuki Unno, Kazuhisa Yuki, Risako Kibushi, Koichi Suzuki, Sanyo-Onoda City University / Japan

OD9: Thermal Management

OD9-1
Relationships of Design Parameters and the Cooling Performance of the Spiral-Fin Heatsink
Shingo Otake[1], Motohito Hori[2], Ryoichi Kato[2], Yoshinari Ikeda[2], Victor Parque[1], Muhammad Khairi Faiz[1], Makoto Yoshida[1], Tomoyuki Miyashita[1], [1]Waseda University, [2]Fuji Electric / Japan

OD9-2
Investigation of Heat Transfer in 3D Packaging for Practical-scale Quantum Annealing Machines
Wei Feng, Katsuya Kikuchi, Mutsuo Hidaka, Hirotake Yamamori, Yuuki Araga, Kazumasa Makise, Shiro Kawabata, National Institute of Advanced Industrial Science and Technology / Japan

WA3-3 (Pre-recorded video for live session presentation)
Parameter Identification of Distributed Thermal Network for Surface Mount Type Power Semiconductor Packages
Koji Nishi, Ashikaga University / Japan

WA3-4 (Pre-recorded video for live session presentation)
Room-Temperature Bonding of AlN Ceramic and Si Semiconductor Substrates for Improved Thermal Management
Takashi Matsumae[1], Yuichi Kurashima[1], Hideki Takagi, Kazunori Nishizono[2], Tsutomu Amano[2], Eiji Higurashi[1], [1]National Institute of Advanced Industrial Science and Technology, [2]MARUWA / Japan

ICEP 2019 Awards

Outstanding Technical Paper Award

"High-Speed High-Density Cost-Effective Cu-Filled Through-Glass-Via Channel for Heterogeneous Chip Integration"

Hiroshi Kudo, Miyuki Akazawa, Shouhei Yamada, Masaya Tanaka, Haruo Iida, Jyunya Suzuki, Takamasa Takano, Satoru Kuramochi, DNP / Japan

"Processing and Characterization of Die-Attach on Uncoated Copper by Pressure-Less Silver Sintering and Low-Pressure-Assisted Copper Sintering"

Meiyu Wang[1], Yanliang Shan[1], Yunhui Mei[1], Xin Li[1], Guo-Quan Lu[1,2], [1]Tianjin University / China, [2]Virginia Tech / USA

"Inhibition of Cracking in Cu6Sn5 intermetallic Compounds at the Interface of Lead-Free Solder Joint by Controlling the Reflow Cooling Conditions"

Flora Somidin[1,2], Stuart D. McDonald[1], Xiaozou Ye[1], Dongdong Qu[1], Keith Sweatman[3], Tetsuya Akaiwa[3], Tetsuro Nishimura[3], Kazuhiro Nogita[1], [1]The University of Queensland / Australia, [2]Universiti Malaysia Perlis / Malaysia, [3]Nihon Superior / Japan

"High-Toughness (111) Nano-Twinned Copper Lines for Fan-Out Wafer-Level Packaging"

Yu-Jin Li[1], Wei-Yu Hsu[1], Benson Lin[2], ChiaCheng Chang[2], Chie Chen[1], [1]National Chiao Tung University, [2]MediaTek / Taiwan

"Programming and Evaluation of a Multi-Axis/Multi-Process Manufacturing System for Mechatronic Integrated Devices"

M. Ankenbrand, Y. Eiche, J. Franke, Fridrich-Alexander University Erlangen-Nuremberg / Germany

ICEP 2019 IEEE EPS Japan Chapter Young Award

"Correlation between Insertion Loss and Interface Relative Conductivity"

Taiga Fukumori, Fujitsu Laboratories / Japan

"Evaluation and Benchmarking of Cu Pillar Micro-Bumps with Printed Polymer Core"

Xing Qiu, Hong Kong University of Science & Technology / Hong Kong

"Cu-Cu Quasi-Direct Bonding with Atomically Thin-Au and Pt Intermediate Layer Using Atomic Layer Deposition"

Hiroyuki Kuwae, Waseda University / Japan

"A Cu-Cu Bonding Method Using Preoxidized Cu Microparticles under Formic Acid Atmosphere"

Runhua Gao, Osaka University / Japan

JIEP Poster Award

"Au-Sn Soldering Using a Micro-heater to Restrain Excess Temperature Rise Inside the Package"

Hideaki Mizusaki, Toshiro Sato, Makoto Sonehara, Shinshu University / Japan

"Wafer-scale Au-Au surface activated Bonding Using Atmospheric-Pressure Plasma"

Michitaka Yamamoto[1,2], Takashi Matsumae[2], Yuichi Kurashima[2], Hideki Takagi[2], Toshihiro Miyake[3], Tadatomo Suga[1], Toshihiro Itoh[1], Eiji Higurashi[1,2], [1]The University of Tokyo, [2]National Institute of Advanced Industrial Science and Technology, [3]Denso / Japan

"Study of Low-Residual Stress Amorphous Film Deposition Method for LiTaO3 / Quartz or LiNbO3 / Quartz Bonding toward 5G Surface Acoustic Wave Devices"

Ami Tezuka[1], Hiroyuki Kuwae[1], Kosuke Yamada[1], Shuichi Shoji[1], Shoji Kakio[2], Jun Mizuno[1,3], [1]Waseda University, [2]Yamanashi University / Japan, [3]Soochow University / China

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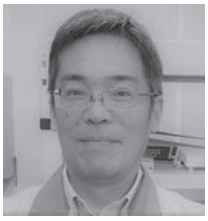

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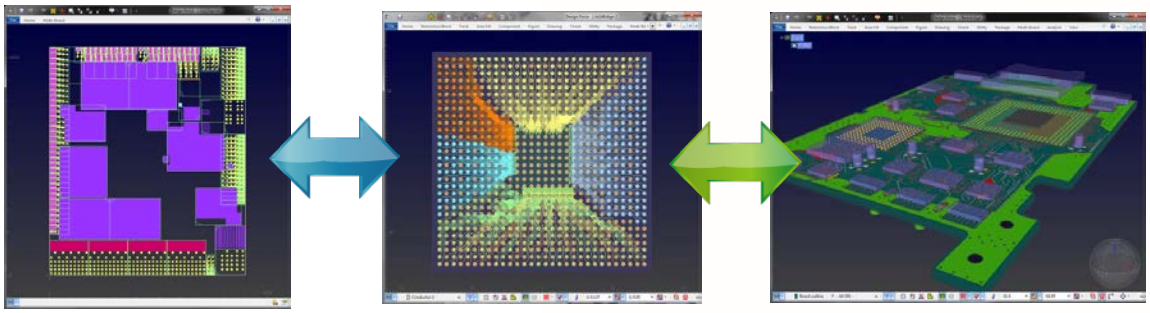
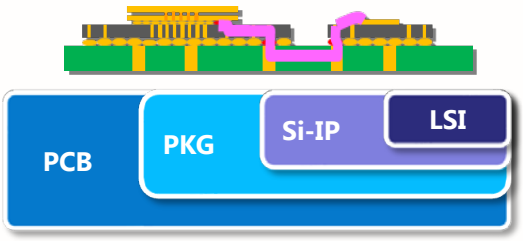
LSI/PKG/Board Co-Design Solution

Design Force

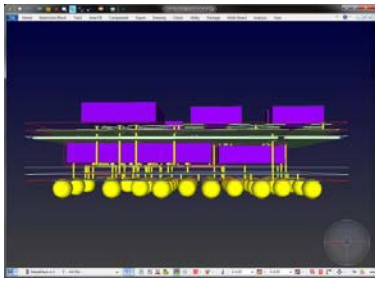
- Support multi-technology & multi-object environment
- Rendering seamless between 2D & 3D technologies
- Optimize I/O of LSI pads and Package pins
- Support the format named Data Format for LSI-Package-Board Interoperable Design
  IEEE Std2401™-2019, IEC 63055



A multi-technology / multi-object environment which shows systems and modules having a complex hierarchical structure, similar to LSI/PKG/PCB, as a single unit is a powerful tool for considering total optimization trade-offs.



SiP / 3DIC



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By Supporting representation of cavity structures in boards and embedded components that are connected to boards at the top and bottom surfaces, and complex designs with combinations of different technologies such as Package on Package, Package in Package, Chip on Board, Board on Board, it contributes to design simplification and efficiency.

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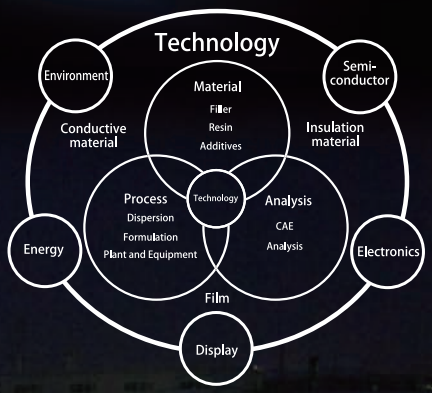
Mutual prosperity to both nature and mankind through Creativity, Innovation and Sensitivity.

In the field of electro-chemical material, NAMICS pursues best product solutions with its advanced technologies and contributes to societies. NAMICS is becoming more and more environmentally-friendly, harmonizing with nature.



Over the past thirty years, the NAMICS CORPORATION has been concentrating on the research, development, manufacture and sale of insulating and conductive materials for electronic components, used in almost every field of the electronic and micro-electronic market needless to mention that we have closely been following the ever-advancing technological trends all the while.
NAMICS' motto in business is to "Satisfy requirements by the customers and market, by offering Quality and Service in the right timing with own unique technologies".
As mentioned above, NAMICS has a great variety of products both for insulating and electro-conductive usages. Our policy is to supply to each customer the tailor-made products.

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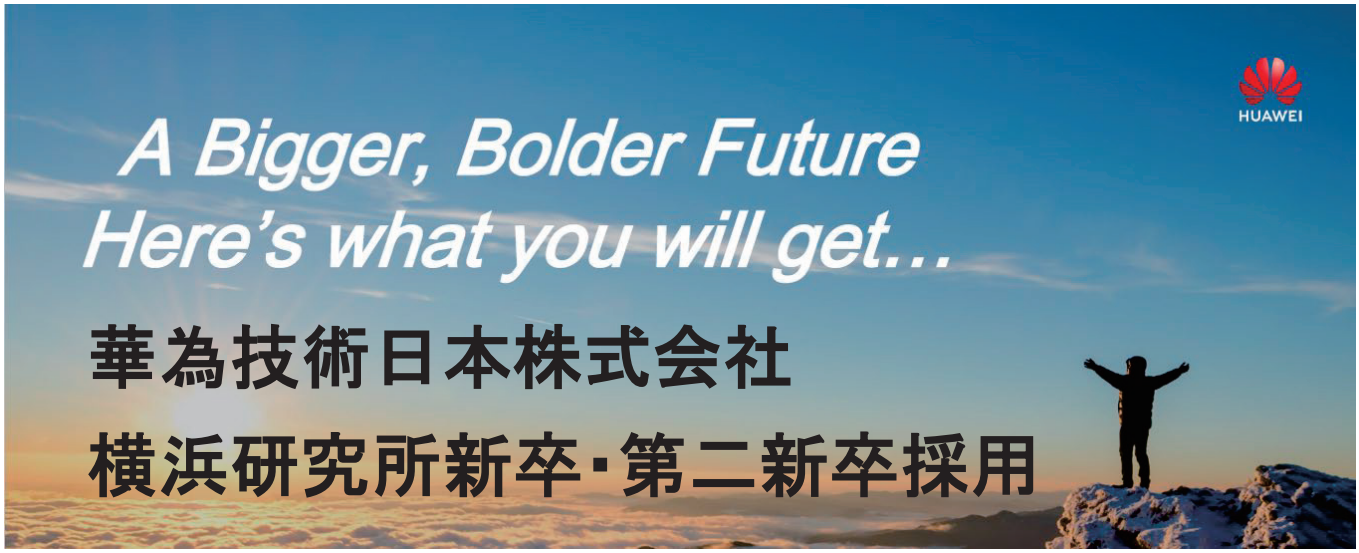

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次世代高密度パッケージ及び実装技術の開発

◆ **高性能誘電材料・プロセス開発**
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◆ **金属材料プロセスエンジニア**
高強度・高耐食性合金材料の原材料の開発、成形プロセスの最適化

◆ **精密駆動機構設計エンジニア**
精密かつ複雑な運動機構の設計、製造加工・精密装置に関する研究

◆ **サーボモータ設計エンジニア**
高性能サーボモータの設計、サーボ制御技術・サーボモータ駆動アルゴリズムの開発

◆ **誘電体・セラミック材料エンジニア**
電子セラミック・マイクロ波誘電体材料配合設計・粉末調製・精密成形・焼結・表面処理などの研究

◆ **有機高分子材料・光学材料エンジニア**
光学材料、接着剤・振動板・キャビティ部品の材料や合成プロセスなど、有機高分子材料の研究開発

【対象】:
博士号取得者・取得予定者（修士号は応相談）
2018年1月～2022年3月に修了（修了予定）の新卒・第二新卒
研究課題が上記いずれかの分野に当てはまる方
仕事で使用できる程度の英語力をお持ちの方

【Contact】: jrrcrecruit@huawei.com

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Yokohama-Japan Research Center, Huawei Technologies CO.,LTD
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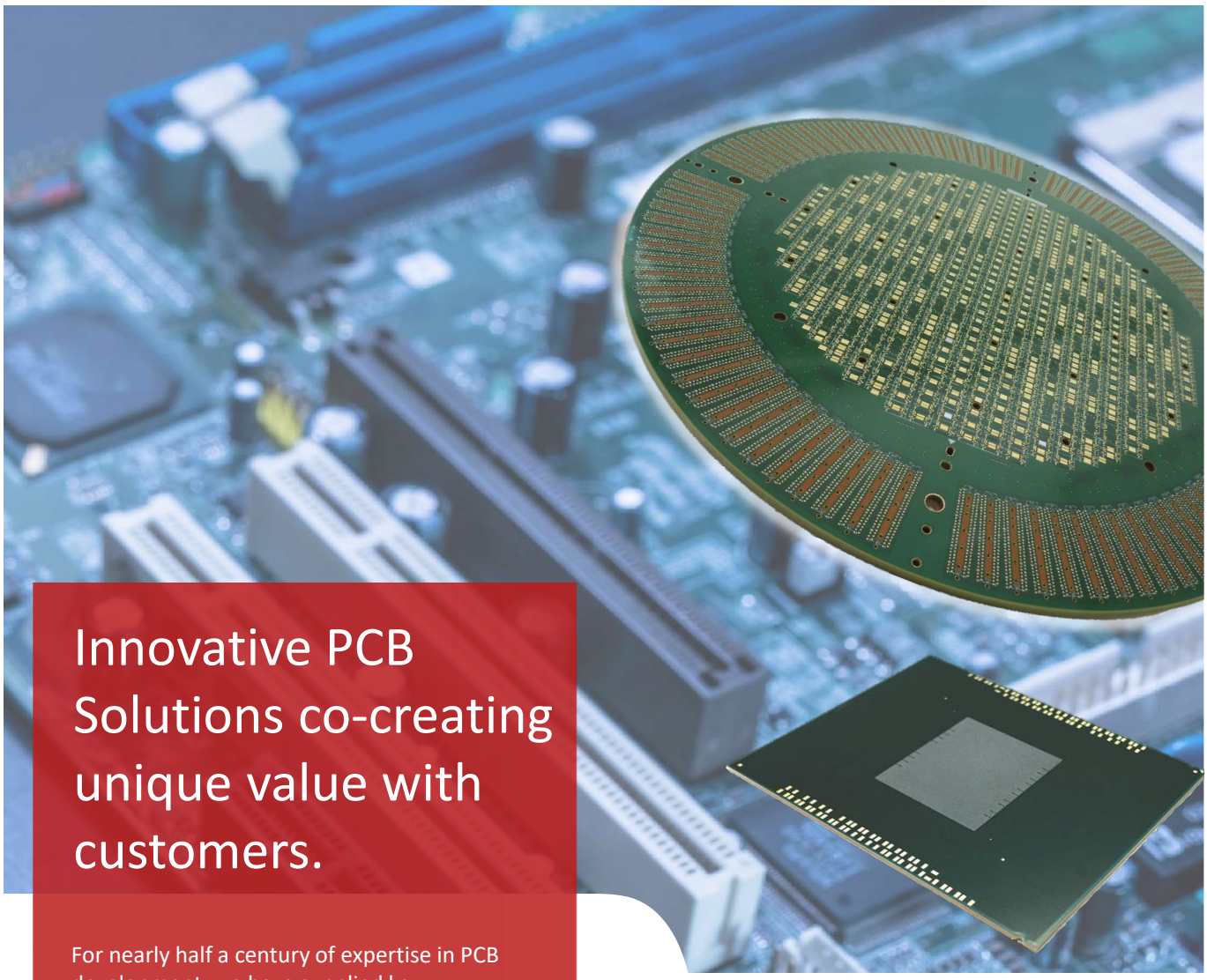
2021年3月現在



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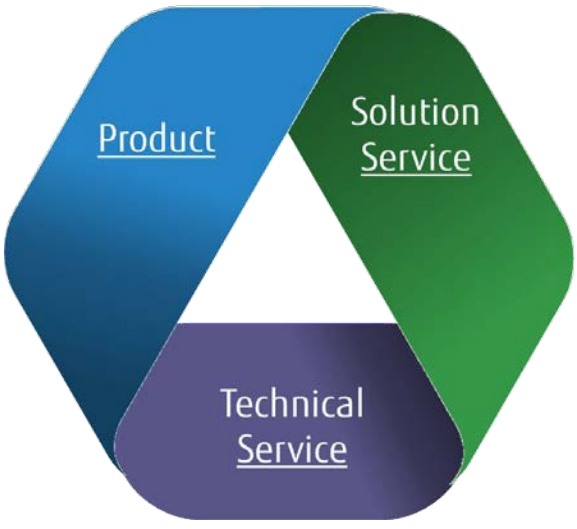
For nearly half a century of expertise in PCB development, we have supplied key components for Supercomputers, ICTs and important public infrastructures.



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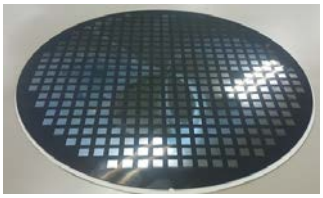
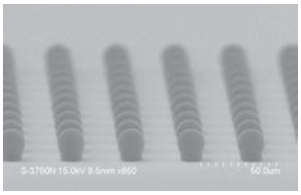
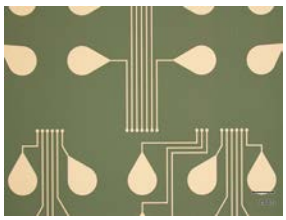
WE ARE PROFESSIONAL IN PROVIDING SEMICONDUCTOR SOLUTIONS

Our FOWLP Solution




Solder Bump formation


Multi Chip package


RDL Process

Semiconductor Market Report

Semiconductor Package business strategy 2021

Semiconductor Production Line Worldwide Annual 2020

FOWLP/FOPLP/ Fronter package market analyze

Matching Site:

SEMI-NET セミネット

https://semi-net.com

Contact to Us

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bondtech

Surface Activated bonding

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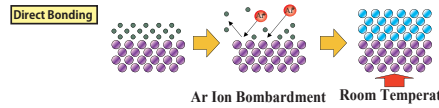
77,Ishiharanishimachi,Kisshoin,Minami-ku,Kyoto
601-8366 Japan
E-mail:yamauchi@bondtech.co.jp

Hybrid Bonding

WOW

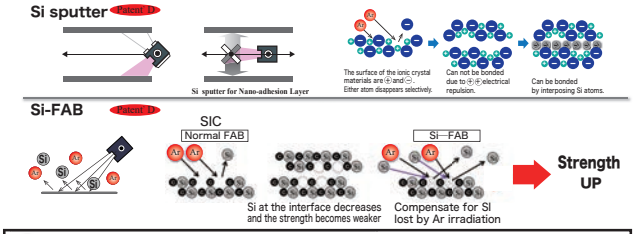
①Room temperature direct bonding in ultra high vacuum



Saw filter, LED,SIC Compaund semiconducter **WF-3000**

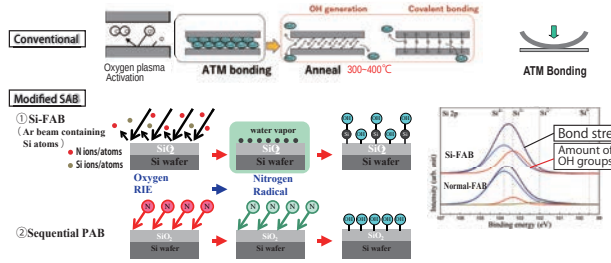
±0.2μm

Machine configuration and bonding process



Ar Bombardment in UHV
- Line type Beam source
- Si sputter
- Si-FAB
  Ar beam containing Si atoms
- 300mm Wafer
  CTC Auto handling
- 6min/wafer

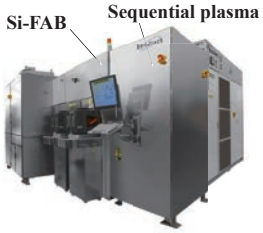
②Hydrophilic bonding in Vacuum



CIS,Memory **WS-3000F**

±0.2μm

- Sequential PAB
- Si-FAB
- 300mm Wafer
  CTC Auto handling
- 15WPH

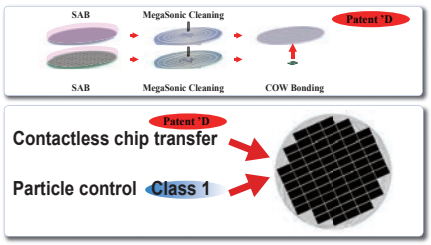


COW

③Surface activated Bonding COW for Semiconductor front end

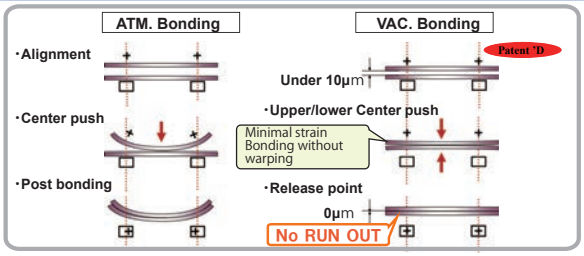
Logic,Memory,CIS

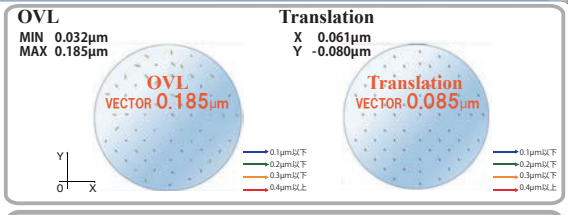
HBCW-3000



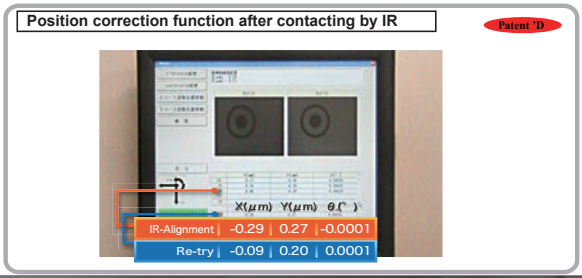
High Accuracy Alignment System

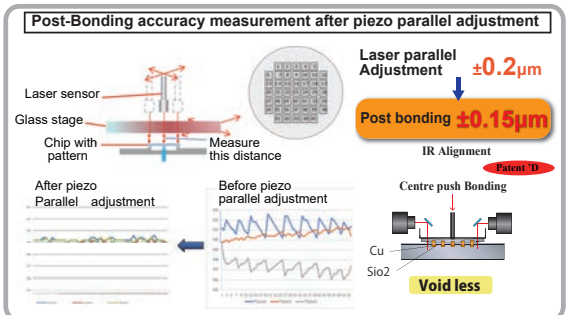
WOW





COW





未来を創る、オンリーワンの研磨技術

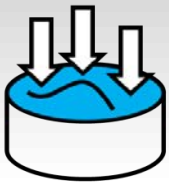
超精密鏡面加工

ティ･ディ･シーの超精密ラップ加工技術により各種ご希望精度を実現

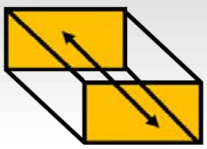
金属、セラミックス、ガラス、半導体、新素材などあらゆる材質に対応

切削、研削、研磨、ポリッシュ等の加工を組み合わせる事により
お客様のご要望に総合的なソリューションを提供します

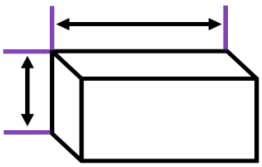
面粗さ:Ra1 nm



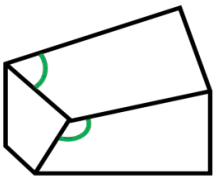
平面度:30 nm



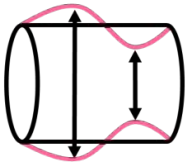
平行度:100 nm



寸法公差:±100 nm



角度:±3秒(1/3600°)



円筒度:500 nm

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Website http://www.mirror-polish.com
Email tdc@mirror-polish.com

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〒981-0113
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湿式比表面積測定装置

Wetted Surface Analyzer

液体に分散されたナノ粒子の比表面積が測定できます

Wetted Surface Analyzer offers wetted surface area measurement of nanoparticles dispersed in liquids

■特長　Features

- パルス NMR による湿式比表面積の測定
  Measurement of wet surface area by Pulse NMR
- 原液での測定
  No dilution
- 予備処理不要
  No preprocessing required
- 簡便・数分で測定可能
  Rapid measurements (Typically minutes)
- 品質管理・研究開発両方で使用できるコンパクトな設計
  Compact design that can be used for both quality control, R&D

■用途　Applications

ナノテクノロジー、医薬品、化粧品、食品、
電子材料、エネルギー、触媒、塗料、インク、
ファインセラミック、高分子など

Nanotechnology, Pharmaceuticals,
Energy, Catalyst, Polymer molecule,
Electronics, Pigments & Coatings,
Fine ceramics　etc.

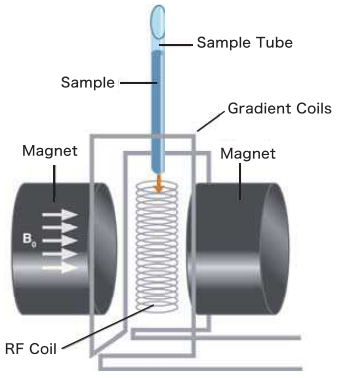
◆粒子比表面積は、粉体原料特性、製造プロセスや製品性能と相関する重要なパラメータです

■測定方法　Measuring Procedure

【測定方法　Measuring Procedure】

1．0.5mlの試料をサンプル管に入れ、装置にセット
Place a 0.5ml sample in a Sample Tube and insert it into the Magnet cassette

2．専用のソフトウエアを使って緩和時間を測定、その結果から粒子比表面積を計算
Measure relaxation time with dedicated software and calculate the surface area of particle from the result



※本装置は、高周波利用設備として所管の総合通信局へ申請が必要です。

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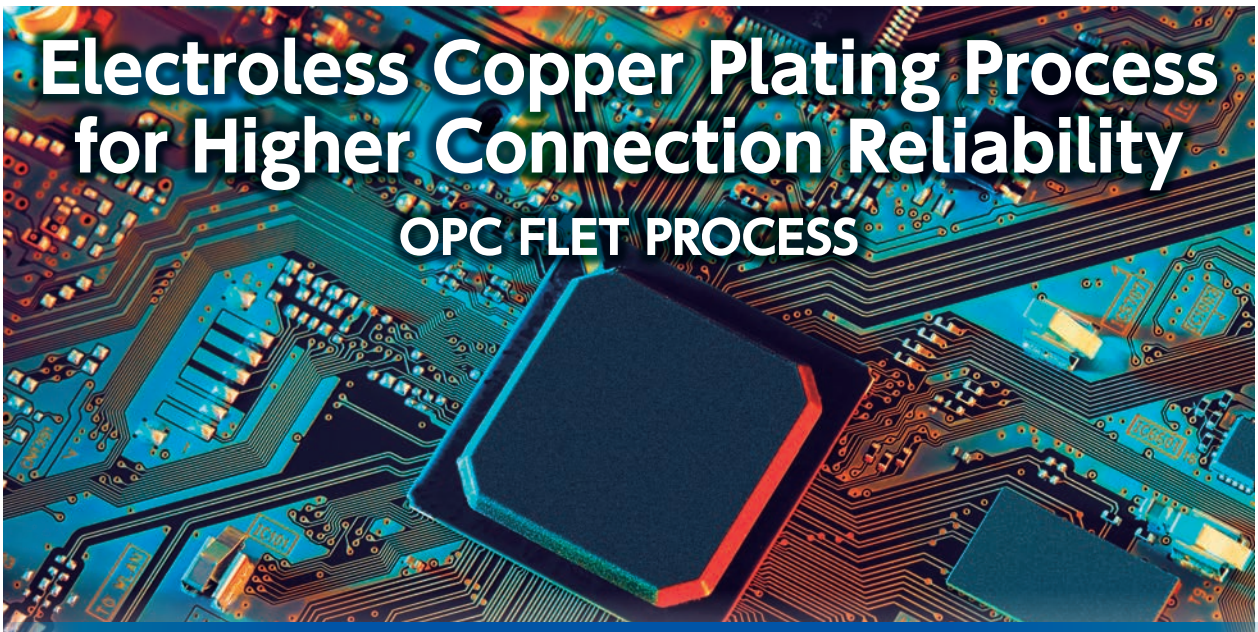
TEL : (077)544-1675/ FAX:(077)544-1698

製造発売者
Xigo Nanotools Inc.（アメリカ）
輸入者
Xigo Nanotools Asia株式会社（日本）

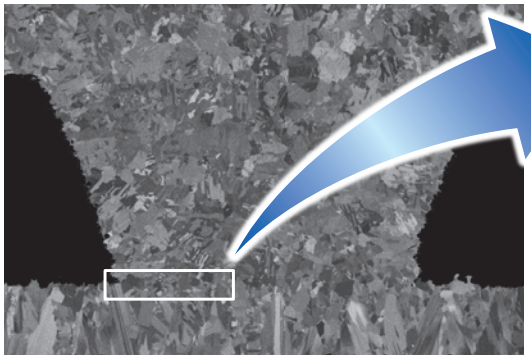
TOP OKUNO

Electroless Copper Plating Process for Higher Connection Reliability

OPC FLET PROCESS

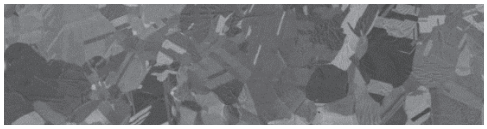


OKUNO supports evolution of semiconductor package substrate



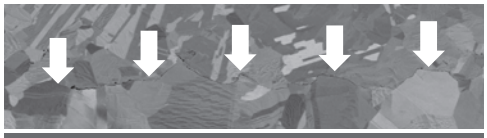
Cross section of via hole

OPC FLET PROCESS



Crystal continuity is observed

Conventional process



No crystal continuity

OKUNO's electroless copper plating process (OPC FLET PROCESS) increases the connection reliability for semiconductor package with high crystal continuity.

奥野製薬工業株式会社 OKUNO CHEMICAL INDUSTRIES CO., LTD.

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1-10-25, Hanaten-higashi, Tsurumi-ku, Osaka, 538-0044, Japan
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Lithography

Etching

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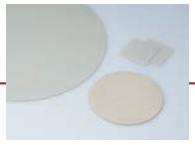
CMP

Precision cleaning and drying of semiconductor wafers and other electronic devices "TOKUSO IPA SE®"

Cleaning

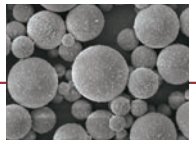
IC chip

Aluminum Nitride (AlN) for Heat dissipation material "SHAPAL™"



Package

High-purity fused spherical silica for EMC filler "EXCELICA®"



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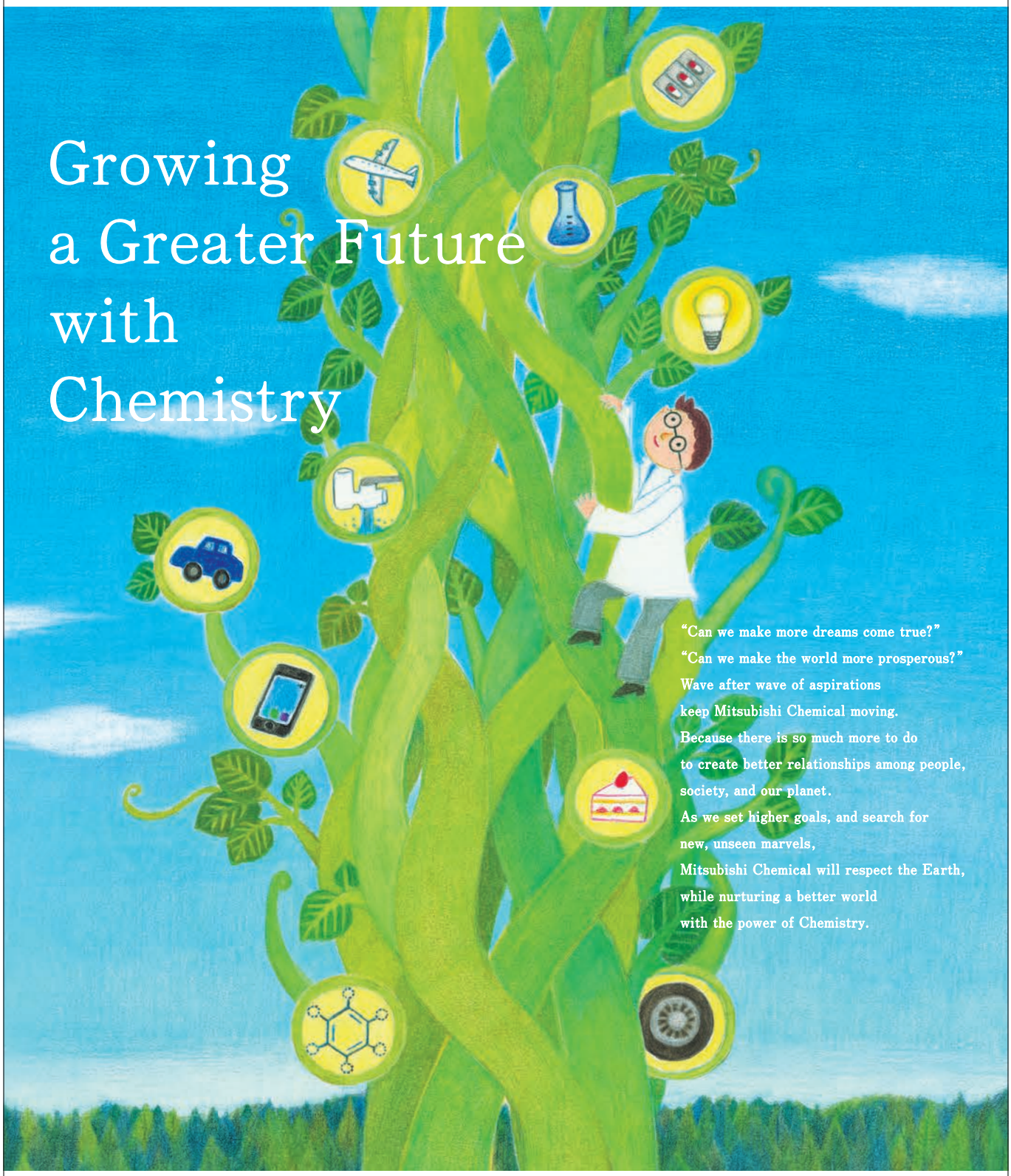
KAITEKI Value for Tomorrow Mitsubishi Chemical Holdings Group



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while nurturing a better world
with the power of Chemistry.

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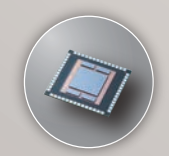
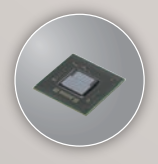
SiP
System-in-Package



2.5D / 3D / TSV



Fan Out

Embedded

Copper Pillar

MEMS

Wirebond

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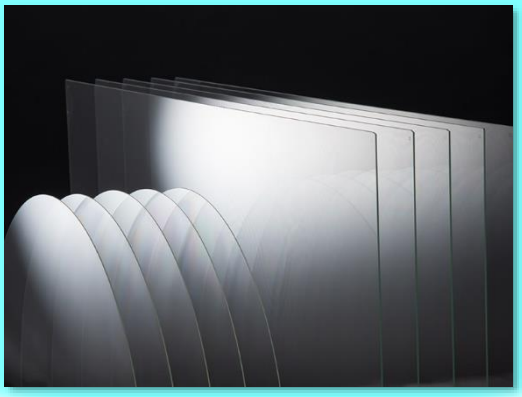
Glass Material Technology

Glass Wafer/Panel for Semiconductor Packaging

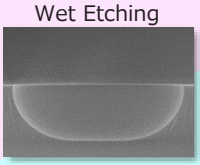
- ✓ High Flatness
- ✓ High Cleanliness of Surface
- ✓ Orientation Flat, Notch, Serially Numbering
- ✓ High Transmittance
- ✓ High Smoothness
- ✓ Edge Treatment with Less Micro Cracks
- ✓ Excellent Electrical Properties



Glass Micro Fabrication Technology

Dry Etching

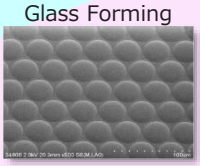
Wet Etching



Nano Imprint

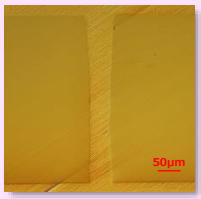
Ultra Thin Glass
(100um thick glass)

Glass Forming



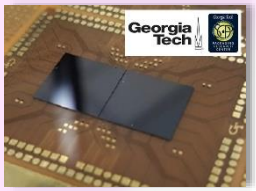
Glass Drilling
(Through Glass Via)

Through Glass Via (TGV)



TGV Panel (~650x550mm)

Glass Substrate



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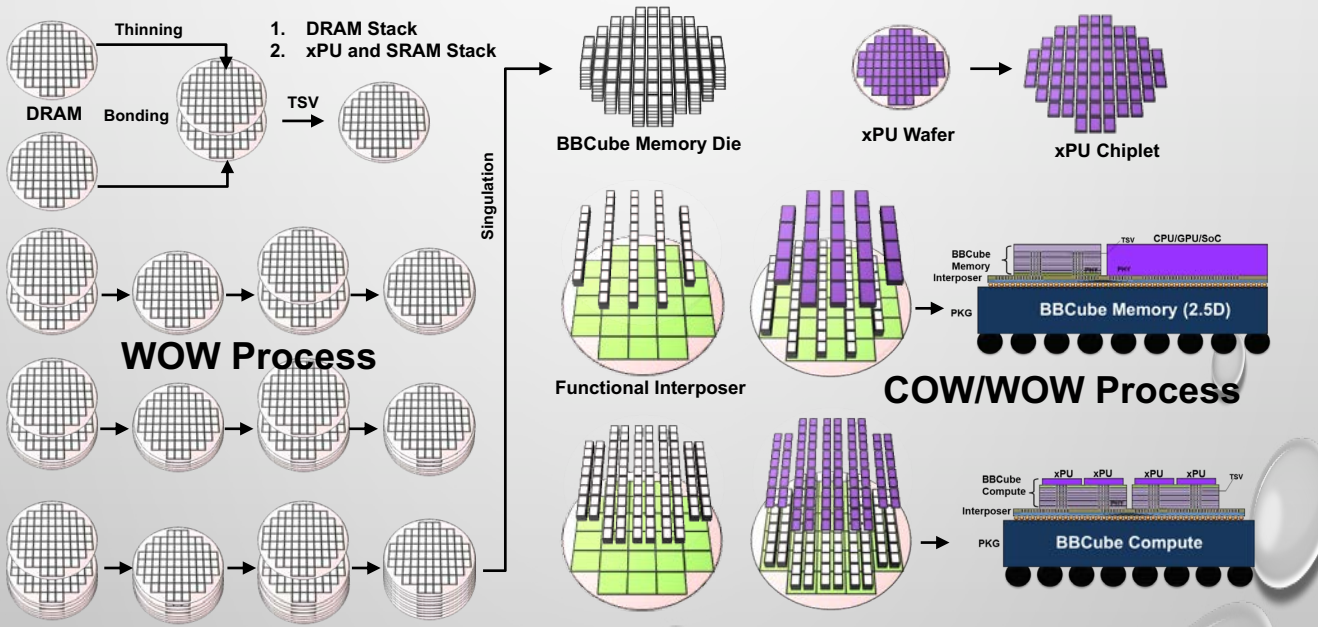

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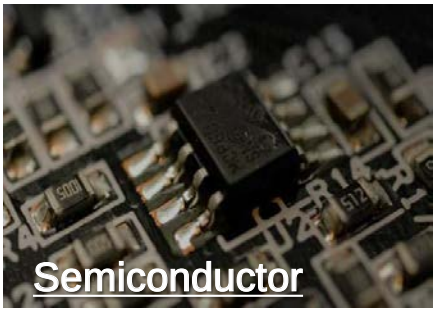
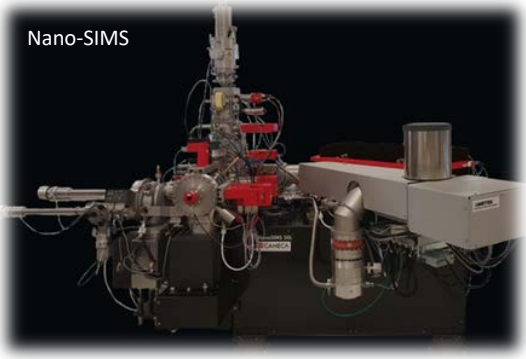
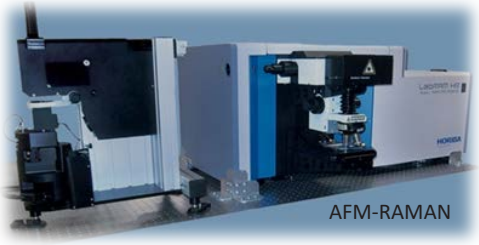




ANALYTICAL EQUIPMENT

- Cs-corrected TEM/STEM
- Dual Beam FIB-SEM
- Nano-SIMS 50L , GCIB TOF-SIMS
- AFM-RAMAN, AFM-IR
- Orbitrap Fusion Lumos
- Spiral TOF MALDI/MS



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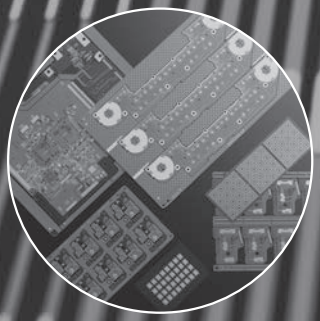
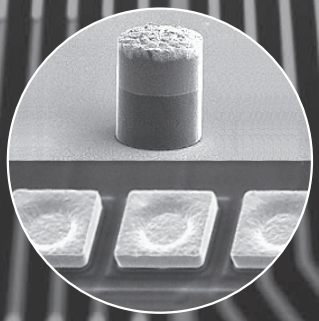
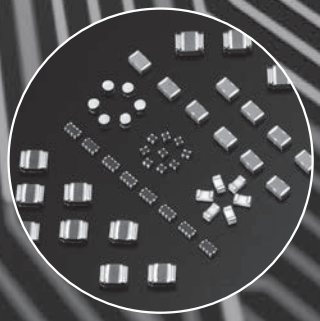


Printed Circuit Boads
- SAP･MSAP
- Au plating(Ep,ELp)
- Cu plating(TH,VF,TF)



Semiconductors
- Bumping survise
- Bump plating
- ELp-UBM plating
- Leadframe



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- Plating for SMD
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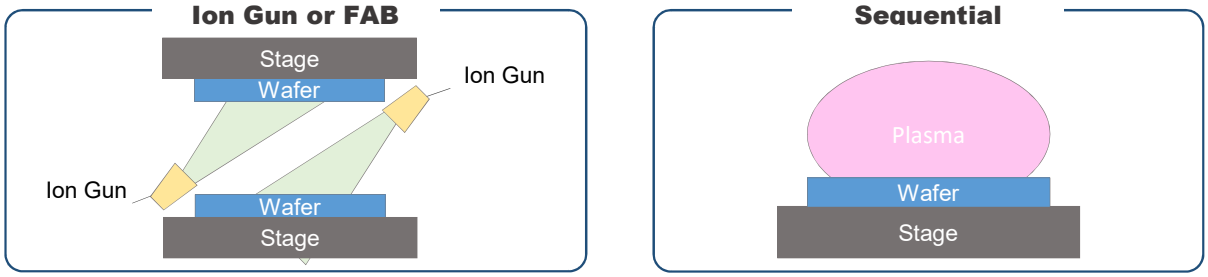
Surface activation wafer bonder

■ROOM TEMPERATURE BONDING with surface activation bonder(SAB)



■Bonde Materials

■Si-Si,Poly Si-Si
■Si-SiO_2/Si
■SiO_2-SiO_2
■Si-SiN/Si
■SiN/SiN
■Glass-Si
■SiC-SiC
■SiC-Si
■LT-Si
■LT-LT
■LN-Si
■LN-SiO_2/Si
■Si-Quartz
■LT--Quartz
■GaAs-Si
■GaAs-GaAS
■GaAs-Gap
■GaP-GaP
■GaN-Sapphire
■GaP-Sapphire
■Si-Sapphire
■GaAs-Sapphire
■ITO-ITO
■Au-Au
■Cu-Cu
■Sapphire-Sapphire
■Sapphire-LT
etc.

■Bonde Materials

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Configuration	Process Chamber(PC)	L/L & PC	L/L & Transfer & PC
Wafer size	2" to 8"	2" to 8"	2" to 8"
Activation source	Ion beam,FAB,Plasma		
Max.Press	100kN		
Vacuum	1×10^{-6}		
Alignment	Wafer edge alignment	Wafer edge alignment	Mark alignment
Alignment accuracy	Less than +/-200um	Less than +/-200um	Less than +/-1um
Bond/batch	1	1	24
Loader	Manual	Manual	Automated(C to C)


SAB-400


SAB-400-Ⅱ


SAB-400-Ⅲ

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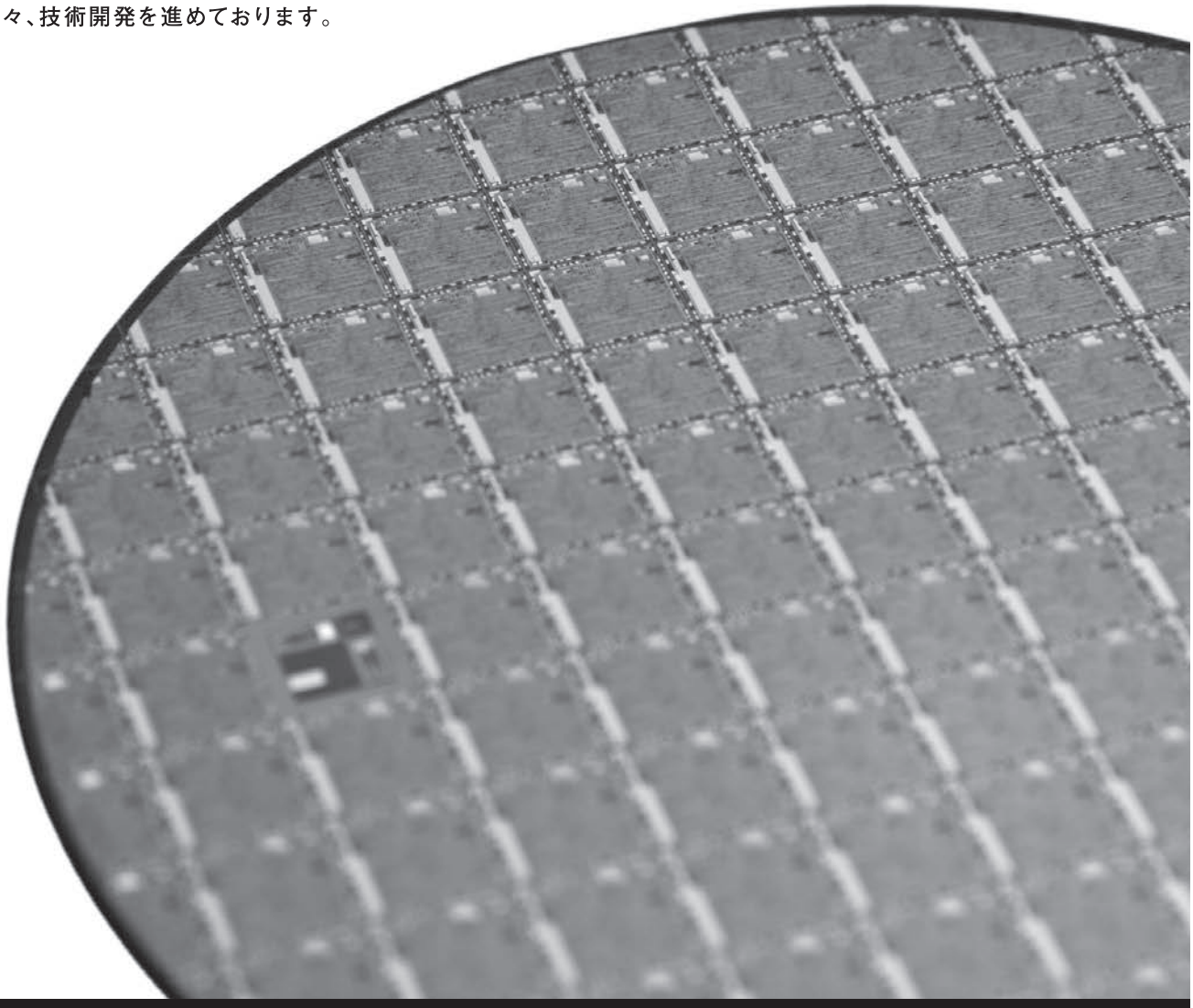

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May 11-13, 2022

2022 International Conference on Electronics Packaging

Venue:

The Sapporo Community Plaza, Hokkaido

General Chair:

Katsumi Miyama

Abstract Submission Deadline:

November 30, 2021

Paper Submission Deadline:

February 28, 2022 ??

May 12, 2021

Edited and Assembled by the Technical Program Committee and the Organizing Committee of
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