Advanced Program

ICEP2010

International Conference on Electronics Packaging

MAY 12 Wed – 14 Fri, 2010

Sapporo Convention Center, Hokkaido, Japan

The International Conference on Electronics Packaging (ICEP) 2010 will be held from May 12th to May 14th at the Sapporo Convention Center in Sapporo, Japan.

This annual conference, launched in 2001, is now in its tenth year. Prior to 2000, we held the IEMT/IMC Symposium four times (1997-2000), following the merger of IEMT (by the IEEE CPMT Society of Japan) and IMC (by the ISHM Japan).

Sapporo is one of the best cities in Japan with its beautiful nature and delicious food. In Sapporo, May is one of the best seasons with the cherry blossoms are in full bloom. Sapporo City is quite accessible for conference participants as several international and domestic air routes are directly connected to New Chitose Airport. From Europe and North America, connections at major international airports in Japan will be required to reach to New Chitose Airport. It takes 36 minutes by airport express train from New Chitose Airport to Sapporo City.

The conference's technical program will include three guest speakers (Professor Shuji Nakamura / University of California, Professor Michael Pecht / University of Maryland and Dr. William T. Chen /ASE Senior Technical Advisor), and 44 technical sessions. The technical sessions include 159 technical papers regarding JISSO technologies such as Advanced Packaging, Substrate, Design and Modeling and Reliability, Manufacturing and Process, Interconnection, Optoelectronics, Printed Electronics, 3D and TSV, MEMS and Sensor, Self-Organization and Self-Assembly, Emerging Technologies, RF, Automotive Electronics, Energy and Environment. 18 posters by university students, who will be the opinion leaders in the future, also are presented.

We plan to hold the welcome reception in the world famous "Sapporo Beer Garden". You can enjoy a night in the beer hall, built of red bricks conveying the era of pioneer days.

The conference will offer you a chance to network with fellow professionals in the field of JISSO technologies and in related fields. We are confident that the conference will provide excellent opportunities for participants to exchange information and network globally. We are looking forward to seeing you at the conference.

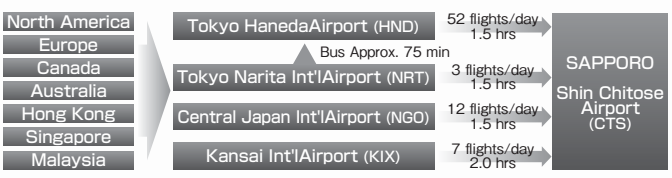
Miki Mori

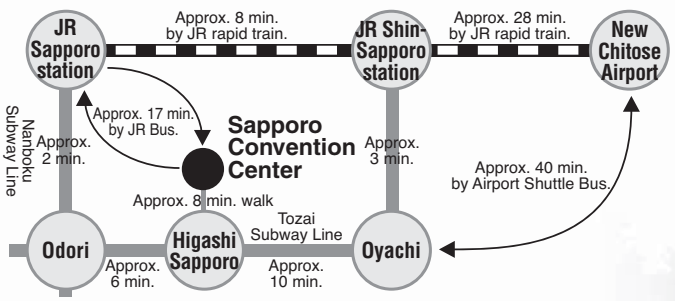
Miki Mori
ICEP 2010 General Chairperson

Sponsored by:
Japan Institute of Electronics Packaging (JIEP)
IEEE CPMT Society Japan Chapter

Contact:
Secretariat of ICEP 2010
JIEP,
3-12-2 Nishiogi-kita, Suginami-ku Tokyo 167-0042, Japan
http://www.jiep.or.jp/icep/

Indirect Flights





Access from the near station

- **If you are coming from Odori or Sapporo Station by Subway.**
  - If you are coming from Odori or Sapporo Station by Subway.
  - Approx. 23 min. from Sapporo Subway Station and approx. 21 min. from Odori Station.
- **If you are coming from the direction of Shin-Sapporo by Subway**
  - Approx. 21 min. from Shin-Sapporo.

Access from New Chitose Airport

- Approx. 60 min. from New Chitose Airport via Sapporo Station.
- Approx. 60 min. from New Chitose Airport via Shin-Sapporo station.

JIEP IEEE CPMT
IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

	Room A (Hall)	Room B (204)	Room C (206)	Room D (207)
10:00	**WA1: LED-1** **WA1-1** <Session Invited> Intelligent Applications of LED Other Than Conventional Uses K.Okamoto, Kagawa University / Japan **WA1-2** <Session Invited> TBD Y.Kawakami, Kyoto University / Japan **WA1-3** <Session Invited> TBD T.-K. Yoo, Lumens / Korea	**WB1: Advanced Packaging-1** **WB1-1** Low Temperature Bonding of Si Wafers in Nitrogen Atmosphere K.Oshikawa, Y.-H.Wang, T.Suga, The University of Tokyo / Japan **WB1-2** Strategies of Aligned Low-Temperature Wafer Bonding for 3D Integration and MEMS C.Wang, T.Suga, The University of Tokyo / Japan **WB1-3** Study on the Warpage Mechanism of Thin Embedded LSI Packages Y.Nakashima, K.Kikuchi, K.Mori, D.Ohshima, S.Yamamichi, NEC / Japan	**WC1: Substrate-1** **WC1-1** Build-up insulator material with a low-dielectric tangent and a low CTE I.Suzuki, Sekisui Chemical / Japan **WC1-2** Novel Thin Copper Transfer Films for Fine Line Formation of PCB Substrates H.Narahashi[1], S.Nakamura[1], T.Yokota[2], [1]Ajinomoto, [2]Ajinomoto Fine-Techo / Japan **WC1-3** High Heat Proofing Naro-Layered Film Cu Wiring by Crystal Grain Growth Control H.Miyagawa, Osaka University / Japan	**WD1: DMR*-1, Reliability** **WD1-1** Viscoelastic finite element simulation of an underfill resin for the reliability evaluation of solder bumps in flip-chip packages A.Yaoita, Toshiba / Japan **WD1-2** The reliability of COG joints fabricated using Sn/Cu bumps and NCAs B.-G.Kim, S.-C.Kim, Y.H.Kim, Hanyang University / Korea **WD1-3** Influence of Inelastic Constitutive Equation on Fatigue Life Prediction of SnAgCu Micro SIder Joint Y.Kanda, K.Zama, Y.Kariya, Graduate School of Shibaura Institute of Technology / Japan
11:15				
	Break			
11:25	**WA2: LED-2** **WA2-1** <Session Invited> Unique High Bright White LED Lens Formation Technology and Its High Reliability Silicone Resin A. Okuno, SANYU REC / Japan **WA2-2** Integrated Enhanced Thermal device of Compact High Power Light Emitting Diode Package C.-J. Weng, Leader University / Taiwan **WA2-3** Optimal Thermal Management of Compact LED Array Backlight Unit of TFT-LCD C.-J. Weng, Leader University / Taiwan	**WB2: Advanced Packaging-2** **WB2-1** Chip-Package Interaction at Advanced Silicon Nodes B.K.Appelt, W.T.Chen, Y.Lai, ASE / USA, Taiwan **WB2-2** Advanced QFN Package for Low Cost and High Performance Solution A.Tseng[1], B.Appelt[1], Y.-S.Lai[2], M.Lin[2], B.Hu[2], JW Chen[2], S.Lee[2], [1]ASE(US), [2]Advanced Semiconductor Engineering / USA, Taiwan **WB2-3** 3D Substrate Innovation for Complex High Pin Count Flip-Chip Applications V.Solberg, V.Oganesian, Tessera / USA	**WC2: Substrate-2** **WC2-1** Two-step plating process in Direct-metallization Y.Morita, Sharp / Japan **WC2-2** Fine circuitry formation on Ar plasma modified polymide layer in a build-up substrate H.Yugawa, Kyocera SLC Technologies / Japan **WC2-3** Metallization technologies onto a smooth resin surface for the next generation packaging M.Horiuchi, T.Yamasaki, Y.Shimizu, Shinko Electric Industries / Japan	**WD2: DMR*-2, Reliability** **WD2-1** Delamination Investigation of Copper Bumps in 3D Chip Stacking Packages Using the Modified Virtual Crack Closure Technique C.J.Wu[1], M.C.Hsieh[2], K.N.Chiang[1], [1]National Tsing-Hua University, [2]Industrial Technology Research Institute / Taiwan **WD2-2** Study on mechanical reliability assessment of multi terminal capacitor assembly on Multi Chip Module K.Okamoto, IBM Japan / Japan **WD2-3** Creep Characteristics of Electrolytic Copper Thin Film H.Kanayama, Ritsumeikan University / Japan
12:40				
	Lunch Time / Poster Session			
13:45	**Welcome Speech** (Room A) M.Mori, General Chairperson Awarding Ceremony Y.Orii, Technical Program Committee Chairperson			
14:15	**Keynote Speech** **Keynote Speech 1** (Room A) GaN-based Solid State Lighting Prof. Shuji Nakamura, University of California			
15:15				
	Break			
15:30	**Keynote Speech 2** (Room A) Does the Electronics Industry Need a New Approach to Qualification? Prof. Michael Pecht, University of Maryland			
16:30	**Keynote Speech 3** (Room A) Engineering in the Year of the Tiger Dr. William T. Chen, ASE(US) Inc.			
17:30				

18:30	**Welcome Reception** (Sapporo Bier Garten)
20:30	

* DMR: Design, Modeling and Reliability

	Room A (Hall)	Room B (204)	Room C (206)	Room D (207)
9:00	**TA1: 3D/TSV-1** **TA1-1** <Session Keynote> Prospect for Development on 3D-Integration Technology and R&D result of Functionally Innovative 3D-Integrated Circuit (Dream Chip) Technology in FY2009 M.Kada, Association of Super-Advanced Electronics Technologies / Japan *(50min)* **TA1-2** Mapping the Customer Landscape; Finding Unmet Needs C.E.Bauer, H.J.Neuhaus, TechLead / USA **TA1-3** 3D integration with TSV interconnects: Technology Trends & Market Analysis J.Baron, Yole Development / France	**TB1: Printed Electronics-1** **TB1-1** <Session Keynote> Ambient Electronics: Print Electronics Everywhere!! T.Someya, The University of Tokyo *(50min)* **TB1-2** <Session Invited> Printed Electronics of Fine Pattern by Inkjet Technology S.Nishi, Konicaminolta IJ Technologies / Japan **TB1-3** <Session Invited> Issues and Approaches Imposed on Ink Jet for The Progress of Printed Electronics M.Fujii, Fuji Xerox / Japan	**TC1: Substrate-3** **TC1-1** Packaging Technology Evolution and Future Low Cost Design Approach and Challenges H.Y.Loo, Intel Microelectronics / Malaysis **TC1-2** Single Sided Substrates - a New Opportunity for Miniaturizing Packages B.K.Appelt, B.Su, A.S.F.Huang, S.Chen, ASE / USA, Taiwan **TC1-3** A Study of Embedded Quad Die In Substrate by Using Au Wire Bonding Method W.-S.Lee, Hynix Semiconductor / Korea **TC1-4** Advanced Embedded Device Substrate with Fine-pitch Metal Circuits Technology T.Tsunoda, Dai Nippon Printing / Japan	**TD1: DMR*-3, Electrical** **TD1-1** Modeling Analysis and Evaluation for Switching Voltage Regulator N.Takahashi, Y.Kosaka, IBM Japan / Japan **TD1-2** Signal Integrity and Power Integrity co-Simulation Correlation Study on the effects of Power Delivery Network Noise to Signal's Performance of Single Ended T.L.Wong, C.C.Lim, Intel Microelectronics / Malaysia **TD1-3** Design optimization on Wirebond package with differential pair signal considering process variations K.Yonehara, IBM Japan / Japan **TD1-4** Application of Low-k Dielectric Materials to Packaging J.Kong[1], Y.-K.Foong[2], C.-S.Lim[2], [1]Intel Microelectronics (M), [2]Universiti Sains Malaysia / Malaysia
10:40				
	Break			
10:50	**TA2: 3D/TSV-2** **TA2-1** Study on System Design-System Integration Method for System LSI Structure H.Murata, Osaka University / Japan **TA2-2** Investigation on the Die Size Effects for Proper 3D-SiP Structure with SDSI Method Y.Iwata, Osaka University / Japan **TA2-3** Vertical Inductor Design with Through Silicon Vias and its Application to 3D Inductive Coupled Standing-Wave-Oscillator M.Shiozaki, A.Iwata, Hiroshima University / Japan **TA2-4** TSV Stress Testing and Modeling M.Amagai, Y.Suzuki, Texas Instruments Japan / Japan	**TB2: Printed Electronics-2** **TB2-1** <Session Invited> Ionic Migration Resistant Wiring Formation by Cu Nanoparticle and Ag-Cu Alloy Nanoparticle Inks M.Nakamoto[1], M.Yamamoto[1], Y.Kashiwagi[1], H.Kakiuchi[2], Y.Yoshida[2], [1]Osaka Municipal Technical Research Institute, [2]Daiken Chemical / Japan **TB2-2** <Session Invited> Low Curing Temperature Ag Nanometalink and Nanometalpaste by Gas Evaporation Method K.Tei, K.Kanazawa, S.Sakio, M.Oda, K.Saitou, ULVAC / Japan **TB2-3** <Session Invited> Inks for Reverse Offset Printing, Useful Tools for Organic TFT M.Kasai, DIC / Japan **TB2-4** <Session Invited> Silver Nano Paste for Printed Electronics Y.Hisaeda, DOWA Electronics Materials / Japan	**TC2: Substrate-4** **TC2-1** High-Permittivity Cu-$BaTiO_3$-epoxy Composites for Embedded Capacitors S.Yu, S.Luo, R.Sun, Chinese Academy of Sciences / China **TC2-2** A Release Property of High-permittivity Thin Film Manufactured with Nano-Transferf Megthod K.Iimura, The University of Tokyo / Japan **TC2-3** Preparation and release property of lead-free dielectric films T.Hosono, The University of Tokyo / Japan **TC2-4** Processing Defects Observation of Multilayered Low Temperature Co-fired Ceramic Substrate R.Alias, S.M.Shapee, Z.M.Yusoff, A.Ibrahim, Z.Ambak, M.R.Saad, TM Research & Development / Malaysia	**TD2: DMR*-4, Mechanical** **TD2-1** Improvement of the accuracy of non-linear finite element analyses of micro electronic packages using the digital image correlation method T.Ikeda[1], T.Kanno[1], N.Shishido[1], N.Miyazaki[1], H.Tanaka[2], T.Hatao[2], [1]Kyoto University, [2]Sumitomo Bakelite / Japan **TD2-2** Study on Resin Crack Prediction Method for Thin and Lead Frame Type Package K.Ashida, Hitachi / Japan **TD2-3** Board Level Validation for Green IC Packaging with Strain-Controllable Dynamic Bending Method J.C.B.Lee[1], C.-K.Yu[1], G.Chang[1], T.Shao[1], X.-K.Meng[2], A.Gallagher[3], [1]IST-Integrated Service Technology, [2]Freescale Semiconductor, [3]Motorola / Taiwan **TD2-4** A Study on Device Simulation Model for the Stress Effects of Semiconductor devices: Device Simulation Using Electron Mobility Model Including Intervalley scattering K.Yoshida, Graduate School of Engineering, Kyoto University / Japan
12:30				
	Lunch Time / Poster Session			
13:30	**TA3: 3D/TSV-3** **TA3-1** <Session Invited> Surface activated bonding of Cu-TSVs and Au stud bumps at room temperature M.R.Howlader, McMaster University / Canada **TA3-2** Process and Applications of Silicon 3D TSV Interposer G.Kim, Kangnam University / Korea **TA3-3** High Throughput Chip on Wafar Assembly Technology and Metallization Reactions of Pb-free micro-joints within a 3DIC Package J.-Y.Chang, S.-Y.Huang, R.-S.Cheng, C.-J.Zhan, T.-C.Chang, Industrial Technology Research Institute / Taiwan **TA3-4** Mechanical Stress and Grain Growth of Cu-Filled Through Sillicon Via H.-Y.Son, G.Lee, M.-S.Suh, Q.-H.Chung, K.-Y.Byun, Hynix Semiconductor / Korea	**TB3: Printed Electronics-3** **TB3-1** <Session Invited> Materials for Printed & Flexible Electronics Device Y.Kumashiro, H.Nakako, M.Inada, K.Kuroda, K.Yamamoto, Hitachi Chemical / Japan **TB3-2** <Session Invited> Chisso's Strategy for Printed Electronics K.Eguchi, Chisso Petrochemical / Japan **TB3-3** <Session Invited> Recent progress on direct patterning process on sub-femt-litter inkjet (Super Ink Jet:SIJ) and electro photography (ZEOMET) K.Murata, National Institute of Advanced Industrial Science and Technology / Japan **TB3-4** <Session Invited> An Organic TFT Backplane using Ink-jet Method and Its Application to a 200ppi Flexible Electronic Paper A.Onodera, Ricoh / Japan	**TC3: Manufacturing Process-1** **TC3-1** Adhesive Copper Seed Layer Formation as an Alternative to Electroless Deposition for Printed Wiring Board Fabrications by Rotation Magnet Sputtering T.Goto[1], O.Kawashima[2], T.Ohmi[1], [1]Tohoku University, [2]Daisho Denshi / Japan **TC3-2** Fabrication of LTCC Substrate Using by Photo Resist Film M.Takatou, Nihon University / Japan **TC3-3** Formation of Fine Circuit Patterns on Cyclo Olefin Polymer Film K.Baba[1], Y.Nishimura[1], M.Watanabe[2], H.Hnma[1], [1]Kanto Gakuin University, [2]Kanto Gakuin Surface Engineering Research Institute / Japan **TC3-4** Study of Oxidation and Reduction Process for Copper Surface with Microwave Plasma A.Takeuchi, T.Kurahashi, K.Takeda, Nissin / Japan	**TD3: DMR*-5, Mechanical** **TD3-1** Heating-Thermometer Device for Evaluation of Thermal Interface Materials M.Kato, Hitachi / Japan **TD3-2** Thermal performance estimation for device embedded substrate K.Ota, Dai Nippon Printing / Japan **TD3-3** Precision Improvement Study of Thermal Warpage Prediction Technology for LSI Packages M.Koide, Fujitsu Advanced Technologies / Japan **TD3-4** Evaluation of Polymer Cure Models in Microelectronics Packaging Applications T.Tilford[1], M.Ferenets[2], P.R.Rajaguru[1], S.Pavuluri[3], M.P.Y.Desmulliez[3], C.Bailey[1], [1]University of Greenwich, [2]Eesti Innovatsiooni Instituut, [3]Heriot-Watt University / UK, Estonia
15:10				
	Break			
15:20	**TA4: Self Assembly-1** **TA4-1** <Session Keynote> Novel Biomimetic Approach for Nano and Micro Patterning of Polymer Materials Based on Self-organization M.Shimomura, Tohoku University / Japan *(50min)* **TA4-2** <Session Invited> Soft and Wet Hydrogel: A Key Material for the Age of Life Science J.P.Gong, Hokkaido University / Japan **TA4-3** <Session Invited> Nanostructure and Surface Function for Self-Assembling N.Saito, Nagoya University / Japan	**TB4: Printed Electronics-4** **TB4-1** <Session Invited> Activity of Program Jisso Consortium, aiming to create commercial prototype using inkjet printing techniques K.Hatada[1], Y.Matsuba[2], K.Oyama[2], N.Terada[2], M.Oda[3], M.Tsubouchi[4], M.Kuchiki[4], H.Tanaka[4], A.Yoshii[5], M.Kitamura[5], K.Sato[6], M.Fukuoka[7], [1]Atomnics Laboratory, [2]Harima Chemical, [3]ULVAC, [4]Kyoritsu Chemical, [5]Namics, [6]Shinko Electronics, [7]Yoneda / Japan **TB4-2** Reading the Fine Print: Challenges and Outlook for Printed Electronics C.E.Bauer, H.J.Neuhaus, TechLead / USA **TB4-3** Low-temperature sintering technique for printable electronic devices M.Yoshida, National Institute of Advanced Industrial Science and Technology / Japan **TB4-4** Novel approach on application manufacturing using inkjet printing, laser ablation and new polymer substrate K.Esa, K.Mikko, K.Satu, R.Pekka, M.Matti, K.Tero, S.Matti, Tanpere University of Technology / Finland	**TC4: Manufacturing Process-2** **TC4-1** Modular Microwave-based System for Packaging Applications R.Adamietz[1], T.Tilford[2], M.Ferenets[3], MPY Desmulliez[4], G.Muller[1], N.Othman[1], F.Eicher[1], [1]Fraunhofer Institut fur Produktionstrchnik und Automatisierung, [2]University of Greenwich, [3]Eesti Innovatsiooni Instituut OU, [4]Heriot-Watt University / Germany, UK, Estonia **TC4-2** Effect of Vacuum Ultraviolet and Formic Acid Treatment for Au-Au Flip Chip Bonding in Three-Demensional (3D) Integrated Structure N.Unami[1], K.Sakuma[1,2], J.Mizuno[1], S.Shoji[1], [1]Waseda University, [2]IBM Japan / Japan **TC4-3** Fine Wire Cu Wire Bonding - the Last Frontier to Reduce Wire Bond Packaging Cost B.K.Appelt, W.T.Chen, A.Tseng, Y.Lai, ASE / USA, Taiwan **TC4-4** Effect of additions of metallic (Ag, Ni) nano particles on the microstructure and shear strength of Sn-Zn solder in ball grid array packages A.K.Gain[1], Y.C.Chan[1], T.Fouzder[2], A.Sharif[3], N.B.Wong[1], W.K.C.Yung[4], [1]City University of Hong Kong, [2]University of Development Alternative, [3]Bangladesh University of Engineering and Technology, [4]The Hong Kong Polytechnic University / Hong Kong, Bangladesh	**TD4: DMR*-6, Thermal** **TD4-1** Study on Loop Heat Pipe Performance related to Electronic Devices T.Takamatsu, K.Hisano, K.Tomioka, H.Iwasaki, Toshiba / Japan **TD4-2** Reduction of Thermal Resistance for Spray Cooling Chip Test Technology by Using Super Thermal Conductivity Material T.Hatakeyama, M.Ishizuka, S.Nakagawa, Y.Hioki, T.Tomimura, Toyama Prefectural University / Japan **TD4-3** Package Embedded Thermal Management Using a Fluidic 3-Dimensional Molded Interconnect Device (3D-MID) T.Leneke, Otto-von-Guericke University of Magdeburg / Germany **TD4-4** Simulation of Through Silicon Via (TSV) Forming with Finite Element Modeling L.Dong, S.W.R.Lee, Hong Kong University of Science and Technology / Hong Kong
17:00				
	Break			
17:10	**TA5: Self Assembly-2** **TA5-1** <Session Invited> Self-assembled Hierarchic Structures of Metal-Molecule Hybrids for Sensing and Electronic Devices K.Ijiro, Hokkaido University / Japan **TA5-2** Micro Bump Formation by Self-Replication Method K.Yasuda, Nagoya University / Japan **TA5-3** Development of Novel Solder Interconnection Technique Using Self Assembly Phenomena of Solder Particles S.Karashima, T.Kitae, S.Sawada, S.Nakatani, T.Ogawa, M.Koyama, S.Matsuoka, Y.Taniguchi, N.Tsukahara, K.Hotehama, Y.Kitade, Panasonic / Japan	**TB5: Printed Electronics-5** **TB5-1** Screen Printing Resolution of Differnt Paste Rheology for Printed Multilayer LTCC Tape S.M.Shapee, R.Alias, A.Ibrahim, Z.Ambak, M.Zulfadli, M.Yusoff, M.R.Saad, M.F.Amiruddin, TM Research & Development / Malaysia **TB5-2** Processing Backplane Technology Development for MEMS Display and New Technology Development of Push-pull Membrane Switch K.Senda, Tokyo University of Agriculture and Technology / Japan **TB5-3** Simple and Low Cost Fabrication of High-Sensitive Capacitance Sensors T.Kasahara[1], M.Mizushima[2], H.Shinohara[1], T.Obata[3], T.Futakuchi[3], J.Mizuno[1], S.Shoji[1], [1]Waseda University, [2]Oga, [3]Toyama Industrial Technology Center / Japan	**TC5: Manufacturing Process-3** **TC5-1** Electromagnetic shield using laminate of copper foil and B -stage epoxy resin A.Kimura, Toshiba / Japan **TC5-2** Dominant Structural Factors of Local Deformation of a Silicon Chip Mounted by Area-Arrayed Flip Chip Structures N.Murata, K.Nakahira. K.Suzuki, H.Miura, Tohoku University / Japan **TC5-3** Intermetallic Growth Rate Effects on Spontaneous Whisker Growth from Tin coating on Copper A.Baated[1], K.-S.Kim[2], K.Suganuma[2], [1]Graduate School of Engineering, Osaka University, [2]Osaka University / Japan	**TD5: DMR*-7, Electrical** **TD5-1** Variation of impedance of two-layered BGA package depending on PCB structure A.Matsuda, Kyoto University / Japan **TD5-2** Impact of Power Plane DC level on Power Referencing Signaling H.C.Shu, C.K.Lee, Intel Microelectronics / Malaysia **TD5-3** Package decoupling cost avoidance through SIPI co-analysis and comprehensive validation M.Chan, Y.H.S.Tau, Intel Microelectronics / Malaysia
18:25				

* DMR: Design, Modeling and Reliability

Room A (Hall)

FA1: Interconnection-1
FA1-1
Development of narrow pitch CSP bonding on FPC
R.Takami, Fujikura / Japan
FA1-2
Hybrid Pad - An Innovative Solution for Flip Chip Ball Grid Array Package Second Level Interconnect Fatigue Life Improvement
E.H.Goh, C.S.Tay, H.N.Chen, J.H.S.Huang, H.T.Teoh, P.T.Oh, T.Keat, Intel Microelectronics / Malaysia
FA1-3
Thermal Fatigue Reliability Studies of Sn-Ag-Cu-Ni BGA Solder Joints on Electroless Ni-P/Au Surface Finish
F.Kawashiro, NEC Electronics / Japan
FA1-4
Influence of additions of ceramic (ZrO_2, Al_2O_3) nano particles on the microstructure and shear strength of Sn-Ag-Cu solder
A.K.Gain[1], Y.C.Chan[1], T.Fouzder[2], A.Sharif[3], N.B.Wong[1], W.K.C.Yung[4], [1]City University of Hong Kong, [2]University of Development Alternative, [3]Bangladesh University of Engineering and Technology, [4]The Hong Kong Polytechnic University / Hong Kong, Bangladesh

10:40

Break

10:50

FA2: Interconnection-2
FA2-1
Microstructural Changes of Micro-joints between Solder and Cu by Electromigration
K.Yasaka, Osaka University Graduate School of Engineering / Japan
FA2-2
Electromigration Study of Nano Ag Doped Lead-Free Sn-58Bi solders on Cu and Au/Ni/Cu Ball Grid Array (BGA) packages
I.Shafiq[1], L.Qingqian[1], T.C.Lam[1], Y.C.Chan[1], N.B.Wong[1], W.K.C.Yung[2], [1]City University of Hong Kong, [2]The Hong Kong Plytechnic University / Hong Kong
FA2-3
Effect of additional Elements on sub-grain structure in Sn-based alloys
A.Yamauchi, Hokkaido University / Japan
FA2-4
Secondary IMC formation induced by Kirkendall voiding in Cu/Sn-3.5Ag solder joints
S.H.Kim, J.Yu, J.Y.Kim, Korea Advanced Institute of Science and Technology / Korea

12:30

Lunch Time / Poster Session

13:30

FA3: Interconnection-3
FA3-1
Electroless Ni/Pd/Au Plating for Semiconductor Package Substrate
Y.Ejiri, Hitachi Chemical / Japan
FA3-2
Electrical Properties of Micro Au Bump Array for Flip-chip Interconnection Made by Electroless Au Plating
F.Kato[1], K.Nomura[1,2], T.Yokoshima[1], S.Nemoto[1], K.Kikuchi[1], H.Nakagawa[1], K.Koshiji[2], M.Aoyagi[1,2], R.Iwai[3], T.Tokuhisa[3], M.Kato[3], [1]National Institute of Advanced Industrial Science and Technology, [2]Graduate School of Science and Technology, Tokyo University, [3]Kanto Chemical / Japan
FA3-3
Surface Activation for Micro-Bumps and Its Improvement on Bonding at Low Temperature
Y.-H.Wang, T.Suga, The University of Tokyo / Japan
FA3-4
Copper Bumping technology for Ultra Fine Pitch Package with C2(Chip Connection) process & Wafer Level Embedded System in Package (WL-eSiP)
I.Kang, NEPES / Korea

15:10

Break

15:20

FA4: Interconnection-4
FA4-1
Unique thermosetting Anisotropic Conductive Ink advanced for fine pitch applications
K.Noguchi, Sanyu Rec / Japan
FA4-2
Aging effects on electrical and thermal conductivitiies of electrically conductive adhesives composed of a heat resistant epoxy binder
M.Inoue[1], H.Muta[1], S.Yamanaka[1], J.Liu[2,3], [1]Osaka University, [2]Chalmers University of Technology, [3]Shanghai University / Japan, Sweden, China
FA4-3
Effect of Flip-Chip Bonding Materials on Reliability of Low-k Semiconductor Devices
T.Nejime, Kyocera SLC Technologies / Japan
FA4-4
Interconnection properties of low-k TEG wafers under stress applied by four-point bending method
M.Masumoto[1], G.Kawashiri[1], Y.Han[2], O.Horiuchi[2], W.Choi[1], H.Tomokage[1], [1]Fukuoka University, [2]Fukuoka Industry, Science and Technology Foundation / Japan

17:00

Room B (204)

FB1: Energy and Environment
FB1-1 <Session Keynote>
Energy, Electronics, and Ecology
C.E.Bauer, H.J.Neuhaus, TechLead / USA
FB1-2 <Session Keynote>
Innovating Our Way to Global Economic Recovery
C.E.Bauer, TechLead / USA
FB1-3
Lead-free plating and whisker growth improvement study
H.Tukiman[1], A.Sriyarunya[2], J.Tondtan[2], [1]Spansion (Kuala Lumpur), [2]Spansion (Thailand) / Malaysia, Thailand
FB1-4
Trace element distribution at the interface of Sn-based solders and Cu substrates
K.Nogita[1], H.Yasuda[2], S.Suenaga[3], H.Tsukamoto[1], C.M.Gourlay[4], S.D.McDonald[1], Y.Suzuki[5], [1]The University of Queensland, [2]Osaka University, [3]Nihon Superior, [4]Imperial College London, [5]SPring-8

FB2: Automotive Electronocs
FB2-1
Lead-free solders for electric vehicles -Global Green Challenge Eco-challenge racing
K.Nogita[1], M.Greaves[2], B.Guymer[2], B.Walsh[2], J.Kennedy[3], T.Nishimura[4], [1]The University of Queensland, [2]Ultramotive Technologies, [3]Tritium, [4]Nihon Superior / Australia, Japan
FB2-2
The Material Deterioration and Microstructure Changes by the Thermal Load and the Effects on the Fatigue Life against Vibration Load
M.Matsushima, Y.Shishihara, H.Matsunami, S.Fukumoto, K.Fujimoto, Osaka University / Japan
FB2-3
A Study on Reliability of Ni Plating in a High Temperature Power Device
T.Ishikawa, Yokohama National University / Japan
FB2-4
Temperatore Development Current Crowding Analysis of Insulated Gate Bipolar Transistor
S.-Y.Chiang, T.-Y.Hung, K.-N.Chiang, National Tsing Hua University / Taiwan

FB3: RF-1
FB3-1
Broadband Feed-through-type Metal-wall package for 50Gbit/s MUX/DEMUX ICs
S.Tsunashima[1], M.Hirata[2], K.Murata[1], [1]NTT, [2]NTT Electronics / Japan
FB3-2
UMB antenna with semicircular and trapezoidal slots on metal housing of electronic equipments
F.Koshiji, K.Sato, The University Tokyo / Japan
FB3-3
Frequency-dependent Characterization of Multi-finger MOSFETs with Different Gate Structures
Y.Song, C.Park, J.H.Kang, I.Yun, Yonsei University / Korea
FB3-4
Implementing DVB-T Modulator on medium size FPGA circuit
M.Maaspuro, University of Turku / Finland

Break

FB4: RF-2
FB4-1
Preliminary Study on High-speed and Long-distance Signal Transmission Combined with Evanescent Wave Energy
K.Hashimoto, K.Kohno, Y.Akiyama, H.Kikuchi, K.Otsuka, Meisei University / Japan
FB4-2
A method of constructing an EMC macro-model LECCS by using Norton's equivalent circuit considering transient current
H.Tanaka, Kyoto University / Japan
FB4-3
The Correlation between Imbalance Current and EM Radiation from a Printed Circuit Board Driven by Differntial-Signaling
Y.Kayano, R.Hashiya, H.Inoue, Akita University / Japan
FB4-4
Specification of the Unnecessary Electro-Magnetic Emission Source and Estimation of Radiation Characteristics in Far Field
T.Watanabe, Aoyama Gakuin University / Japan

Room C (206)

9:25

FC1: MEMS-1
FC1-1 <Session Invited>
Heterogeneous Integration of Micro-optics for Optical Microsensors
E.Higurashi, The University of Tokyo / Japan
FC1-2
Pressure Measurement based on Photothermal Excitation and Interferometric Detection of Micro-cantilevers for Micro-device Packaging
S.Yamamoto, The University of Tokyo / Japan
FC1-3
Low-temperature wafer bonding for MEMS hermetic packaging using sub-micron Au particles
H.Ishida, SUSS Micro Tec / Japan

FC2: MEMS-2
FC2-1 <Session Invited>
Integration of Polymer Material in MEMS Devices
N.Miki, Keio University / Japan
FC2-2
Fabrication of Polymer Micro Needle Arrays
Y.Ami, N.Miki, Keio University / Japan
FC2-3
Integration method of bridging-structural CNTs into Si wafer by stamping transfer
Y.Takei, The University of Tokyo / Japan
FC2-4
How scientific knowledge influence the market growth ; Study on the correlation between the MEMS study and mmarket
K.Shinagawa, S.Hirokawa, Y.Muto, Canon Marketing Japan / Japan

FC3: Manufacturing Process-4
FC3-1
Precise Structure Controlled Plastic Hot Embossing Method for Low-temperature Direct Bonding
H.Shinohara, J.Mizuno, S.Shoji, Waseda University / Japan
FC3-2
Studies on direct bonding of PDMS with PC, COP and PMMA using pretreatment of atmospheric-pressure oxygen plasma
S.Matsui, H.Shinohara, J.Mizuno, S.Shoji, Waseda University / Japan
FC3-3
High-speed Laser Plating for Wire-Bonding Pad Formation
K.Maekawa, Ibaraki University / Japan
FC3-4
Modeling of Tapered Reactive Ion Etching Process of SiO_2 Layer using Neural Networks
P.Moon, Y.Lee, C.E.Kim, J.Seo, T.Lee, I.Yun, Yonsei University / Korea
FC3-5
Modeling of Amorphous InGaZnO TFTs with Channel Width and Length Variation
E.N.Cho, J.H.Kang, Y.Song, I.Yun, Yonsei University / Korea

15:35-15:45 **Break**

FC4: Substrate-5
FC4-1
The study of CAF property less than 130μm pitch vias by laser driling
H.Murai, Hitachi Chemical / Japan
FC4-2
Effect of Inorganic Fillers on Properties of Printed Circuit Board
C.-J.Lai, Wuxi Grace Electeon Technology / China
FC4-3
Hot Air Solder Levelling in the Lead-Free Era
K.Sweatman, Nihon Superior / Japan

Room D (207)

FD1: DMR*-8, Electrical
FD1-1
Experiment investigation of the performance of DDR3 DRAM packages
R.Crisp[1], W.-J.Fan[2], W.Chang[2], A.Chang[2], [1]Tessera, [2]Powertech Technology / USA, Taiwan
FD1-2
A Method for Reducing the Number of the Metal Layers for Embedded LSI Package
D.Ohshima, K.Mori, Y.Nakashima, K.Kikuchi, S.Yamamichi, NEC / Japan
FD1-3
Built-in Test Circuit for Opens at Interconnects betweden Dies inside SiPs
M.Hashizume, The University of Tokushima / Japan
FD1-4
Faulty Effects on Logic Signal of a Hard Open Via from Adjacent Ones
K.Manabe, Kagawa National College of Technology / Japan

FD2: DMR*-9, Electrical
FD2-1
Current Carrying Capability of Fine Pitch Compliant Bumps on COG Packaging
C.-C.An, Industrial Technology Research Institute / Taiwan
FD2-2
Power Delivery Network Design for Complex Low Cost Chip
A.S.Chai, H.C.Shu, Intel Microelectronics / Malaysia
FD2-3
SRAM Core Modeling Methodology for Efficient Power Delivery Analysis
F.N.Tan, S.G.Pang, C.L.Ng, K.Y.Wong, L.K.Yong, Intel Microelectronics / Malaysia
FD2-4
Characterization and modeling of the Power delivery networkws of High Speed I/O Buffer
F.N.Tan, L.C.Quek, Intel Microelectronics / Malaysia

FD3: Optoelectronics-1
FD3-1
Graded Index Core Polymer Parallel Optical Waveguide and Its Crosstalk Analysis
H.-H. Hsu, Keio University / Japan
FD3-2
On-board Faburication of Polymer Parallel Optical Waveguide with Graded Index Cores
Y.Nitta, Keio University / Japan
FD3-3
Polymer Optical Waveguide with Tapered Thickness enabling Larger Positional Tolerance
N.Ishizawa[1], M.Kanda[1], O.Mikami[1], T.Shioda[2], [1]Tokai University, [2]Mitsui Chemicals / Japan
FD3-4
Wavelength addressing optical interconnection between optical waveguide channels using passive alignment technique by a micro hole array
K.Nakama, Y.Tokiwa, O.Mikami, Tokai University / Japan

15:10-15:20 **Break**

FD4: Optoelectronics-2
FD4-1
Hetero-integration of High Doped Silicon micro wire to III-V Active Layer for Electrical Pumping Light Emission by Plasma Assisted Bonding
L.-H.Li, A.Higo, R.Takigawa, E.Higurashi, M.Sugiyama, Y.Nakano, The University of Tokyo / Japan
FD4-2
Radiation cooling effects on recent advanced electronic device performances with alumina heat sinks of high infrared emmisivity material
K.Shinagawa[1], M.Nishimura[2], S.Hirokawa[1], Y.Muto[1], [1]Canon Marketing Japan, [2]Nishimura Porcelain / Japan
FD4-3
Solvents Effect on Morphology and Structure of Semi-conductive Poly (9, 9-di-n-octyl-2,7-fluorene) (PFO) Film
Z.Y.Ke[1], H.C.Chen[1], C.L.Chung[1], S.L.Fu[1], C.Y.Ou[2], [1]I-Shou University, [2]Research Alliance Taiwan TFT LCD Association / Taiwan

16:35

* DMR: Design, Modeling and Reliability

■Session;

Invited Speeches

GaN-based Solid State Lighting

Prof. Shuji Nakamura
University of California

The high efficiency of blue LEDs and white LEDs would save significant energy and resources. The U.S. Department of Energy estimates that up to $98 billion USD in energy costs could be saved by 2020 if we switch to solid state lighting. Also, this would reduce the associated greenhouse gas emission, therefore it could reduce global warming effects dramatically. This would help all countries achieve reduced emissions in accordance with the Kyoto Protocol. The current efficiency of white LEDs is around 50% under the R&D level. In order to increase the efficiency of white LEDs further, we would have to increase the light extraction efficiency and the internal quantum efficiency of the LEDs. The packaging technology is directly related with the light extraction efficiency. The nonpola/semipolar GaN technology is directly related with the internal quantum efficiency. Here, the current status of nonpolar/semipolar LEDs and LDs are described.

We reported the fabrication of violet InGaN/GaN Light Emitting Diodes (LEDs) on the first nonpolar m-plane $(1\bar{1}00)$ GaN bulk substrates in 2007. The output power and External Quantum Efficiency (EQE) at a driving current of 20 mA were 28 mW and 45% respectively, with peak electroluminescence (EL) emission wavelength at 400 nm. Also, we fabricated high-efficient nonpolr/semipoalr blue, green and yellow LEDs. The first nonpolar m-plane $(1\bar{1}00)$ nitride laser diodes (LDs) were realized on low extended defect bulk m-plane GaN substrates. We succeeded in fabricating a nonpolar pure blue laser diode under room-temperature CW operation. For green laser diodes, we fabricate a semipolar 513nm pulsed operation green laser diode recently.

■Biography

Shuji Nakamura was born on May 22, 1954 in Ehime, Japan. He obtained B.E., M.S., and Ph.D. degrees in Electrical Engineering from the University of Tokushima, Japan in 1977, 1979, and 1994, respectively. He joined Nichia Chemical Industries Ltd in 1979. In 1988, he spent a year at the University of Florida as a visiting research associate. In 1989 he started the research of blue LEDs using group-III nitride materials. In 1993 and 1995 he developed the first group-III nitride-based blue/green LEDs. He also developed the first group-III nitride-based violet laser diodes (LDs) in 1995. He has received a number of awards, including: the Nishina Memorial Award (1996), MRS Medal Award (1997), IEEE Jack A. Morton Award, the British Rank Prize (1998) and Benjamin Franklin Medal Award (2002). He was elected as the member of the US National Academy of Engineering (NAE) in 2003. Also, he received the Millennium Technology Prize in 2006. Since 2000, he is a professor of Materials Department of University of California Santa Barbara. He holds more than 100 patents and has published more than 390 papers in this field.

Does the Electronics Industry Need a New Approach to Qualification?

Prof. Michael Pecht
University of Maryland

The electronics market has changed dramatically over the past twenty years.
Companies are now in competitive struggle to make smaller products with more functions and less cost. The competition for product differentiation is also intense and the supply chain for products has become more diffused and complex. This is all further complicated by environmental regulations.

To be competitive, companies face the conundrum of having to supply reliable products while reducing time to market and offering competitive pricing. A costly and lengthy part of the product development process is qualification; the process of demonstrating that a product is capable of meeting or exceeding specified requirements. On the other hand, there are many recent examples of huge recalls resulting from poor product qualification.

This presentation will discuss the challenges being faced to qualify products today and provides suggestions for a new approach to qualification.
The goal of this presentation is to provide industry a means to meet customer requirements and at the same time remain cost and schedule competitive.

■Biography

Professor Michael Pecht is currently a visiting Professor in Electronic Engineering at City University in Hong Kong. He has an MS in Electrical Engineering and an MS and PhD in Engineering Mechanics from the University of Wisconsin at Madison. He is a Professional Engineer, an IEEE Fellow, an SAE Fellow, an ASME Fellow and an IMAPS Fellow. He was awarded the highest reliability honor, the IEEE Reliability Society's Lifetime Achievement Award in 2008. He has previously received the European Micro and Nano-Reliability Award for outstanding contributions to reliability research, 3M Research Award for electronics packaging, and the IMAPS William D. Ashman Memorial Achievement Award for his contributions in electronics reliability analysis. He served as chief editor of the IEEE Transactions on Reliability for eight years and on the advisory board of IEEE Spectrum. He is chief editor for Microelectronics Reliability and an associate editor for the IEEE Transactions on Components and Packaging Technology. He is the founder of CALCE (Center for Advanced Life Cycle Engineering) at the University of Maryland, which is funded by over 150 of the world's leading electronics companies at more than US$6M/year. He is also a Chair Professor in Mechanical Engineering and a Professor in Applied Mathematics at the University of Maryland. He has written more than twenty books on electronic products development, use and supply chain management and over 400 technical articles. He consults for 22 major international electronics companies, providing expertise in strategic planning, design, test, prognostics, IP and risk assessment of electronic products and systems.

Engineering in the Year of the Tiger

Dr. William T. Chen
ASE (US) Inc.

The world economy has experienced the worst economic depression of all time. The electronic industry, an integral part of the global economy, has not escaped the trauma of economic contraction and growth. In this Year of the Tiger, the economy is recovering, and the electronics market is brimming with new and exciting electronic products for the ever-more connected world. Since the invention of transistor some sixty odd years ago, the progress of electronics has been paced by Moore's Law, and packaging has been an important contributor. With the ascendency of the consumer market, the function and realm of electronic products has increased many fold, meaning speed and performance are no longer the sole drivers. In this era of More Moore and More than Moore, packaging technology has become the critical enabler for the electronics industry. For packaging engineering professionals, the last decade has been a period of blossoming for many innovations and steady technology advancements. And the pace had not slackened. Cu wirebond is infiltrating the gold wirebond space, traditionally occupied by gold since the invention of integrated circuits some sixty years ago. Flip chip CSP and Wafer level CSP are becoming mainstream. The world of 3D packaging is evolving in measured pace towards wafer level fan-out and 3D IC. Are they real disruptive technologies? And an equally relevant question is - disruptive for whom? This talk will examine the market landscape and technology trends from the perspective of packaging engineers, and ask a different and crucial question "how will the engineering be done in the Year of the Tiger?"

■Biography

William Chen (Bill) currently holds the position of Senior Technical Advisor at ASE (U.S.) Inc. Prior to joining the ASE Group, Bill was Director of the Institute of Materials Research & Engineering (IMRE), located in the National University of Singapore. He was also a Principal Research Fellow at IMRE. Previously, Bill worked for over thirty three years performing various R&D and management positions at IBM Corporation, where he was elected to the IBM Academy of Technology. He is currently the co-chair of the International Technology Roadmap for Semiconductors (ITRS) Assembly and Packaging International Technical Working Group. Bill has been an associate editor of the IEEE/CPMT transactions, and ASME Journal of Electronic Packaging, and has published extensively in the fields of microelectronics packaging and mechanics of materials. He held the position of President of the IEEE Components Packaging and Manufacturing Technology Society (CPMT) from 2006-2009. Bill has been elected a Fellow of IEEE and a Fellow of ASME.

Bill held adjunct faculty appointments at Cornell University, Binghamton University, University of Washington, and a visiting faculty appointment at Hong Kong University of Science of Technology. He received his B.Sc. at University of London, M Sc at Brown University and PhD at Cornell University.

Oral Session

3D/TSV / Advanced Packaging / Automotive Electronics / DMR*, Electrical / DMR*, Mechanical / DMR*, Thermal / DMR*, Reliability / Energy and Environment / Interconnection / LED / Manufacturing Process / MEMS / Optoelectronics / Printed Electronics / RF / Substrate / Self Assembly

* DMR: Design, Modeling and Reliability

Poster Session

P001 The Method of Multi Die Stacking by self alignment
M.Jeong, Y.Lee, C.Lee, W.Shin, J.Bae, H.Jeong, Pusan National University / Korea

P002 The Research of Iterative Learning Control Method on Linear Voice Coil Motor and Application in Flip Chip
H.-C.Qin, Huazhong University of Science & Technology / China

P003 A Processor with Dynamically Reconfigurable Circuit for Floating-Point Arthmetic
Y.Minagi, Tokyo Denki University / Japan

P004 Volume Fraction of β-Sn in Sn-Ag or Sn-Cu Hyper-Eutectic and Eutectic Alloys
Y.Takamatsu, H.Esaka, K.Shinozuka, National Defence Academy / Japan

P005 Effect of cooling rate and composition on solidification process with crystallization in Sn-Ag-Cu alloys
S.Kirai, Hokkaido University / Japan

P006 Effect of Additional Elements on Corrosion Resistance of Carbon Steel in Molten Lead-free solder
T.Kawamoto, Hokkaido University / Japan

P007 Influences of the electroless nickel film condition for the electroless Au/Pd/Ni film property
I.Kato[1], T.Kato[1], H.Terashima[2], H.Watanabe[2], H.Honma[1], [1]Kanto Gakuin University, [2]Kojima Chemicals / Japan

P008 Impact test of Sn-3.0Ag-0.5Cu (-xCo) solder with Co-P plating
T.Daito[1], H.Nishikawa[1], T.Takemoto[1], T.Matsunami[2], [1]Osaka University, [2]Okuno Chemical Industries / Japan

P009 Self-Organized Dots Formation on Si Substrate by Nd: YAG Laser
Y.Yoshida[1], S.Kayashima[1], S.Yatsu[1], S.Watanabe[1], M.Kawai[2], T.Kato[3], [1]Hokkaido University, [2]KEK, [3]Hitachi / Japan

P010 Modification of Self-Organized Chemical Bonding Structure of Hydroganated Amorphous Carbon using Si Doping
S.-M.Baek, T.Shirafuji, S.-P.Cho, N.Saito, O.Takai, Nagoya University / Japan

P011 Creation of Super Hydrophobic Inner Surface of Narrow Tubes by ICP-CVD Using Trimethylmethoxysilane
Y.Takahashi[1], T.Shirafuji[1], N.Saito[1,2], O.Takai[1,2], [1]Nagoya University, [2]CREST / Japan

P012 Effect of Solution pH on Silica Fabrication by Solution Plasma Process
T.Yamamoto[1], J.Hieda[1], N.Saito[1,2], O.Takai[1,2], [1]Nagoya University, [2]CREST / Japan

P013 Solution Plasma Processing of Nano Carbon Materials and its Effects on Their Self-Organized Dispersion in Plastic Materials
Y.Noguchi[1], T.Shirafuji[1], N.Saito[1,2], O.Takai[1,2], [1]Nagoya University, [2]CREST / Japan

P014 Synthesis and structure evaluation of ZrO_2 nano-particles prepared by solution plasma
K.Suzuki, Nagoya University / Japan

P015 MEMS-based hydraulic displacement amplification for tactile displays applications
X.Arouette, Y.Matsumoto, T.Ninomiya, Y.Okayama, NiMiki, keio University / Japan

P016 Development of Distributed Capacitive Sensor with Encapsulated Ferroelectric Liquid
Y.Hotta, Keio University / Japan

P017 Development of a Micro-scale Biomimetic Tactile Sensor with Epidermal Ridges for High Sensitivity
Y.Zhang, T.Maeno, N.Miki, Keio University / Japan

P018 TCP/IP body-centric network in intra-body communication
F.Koshiji, S.Takenaka, T.Maesaka, K.Sasaki, The University of Tokyo / Japan

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